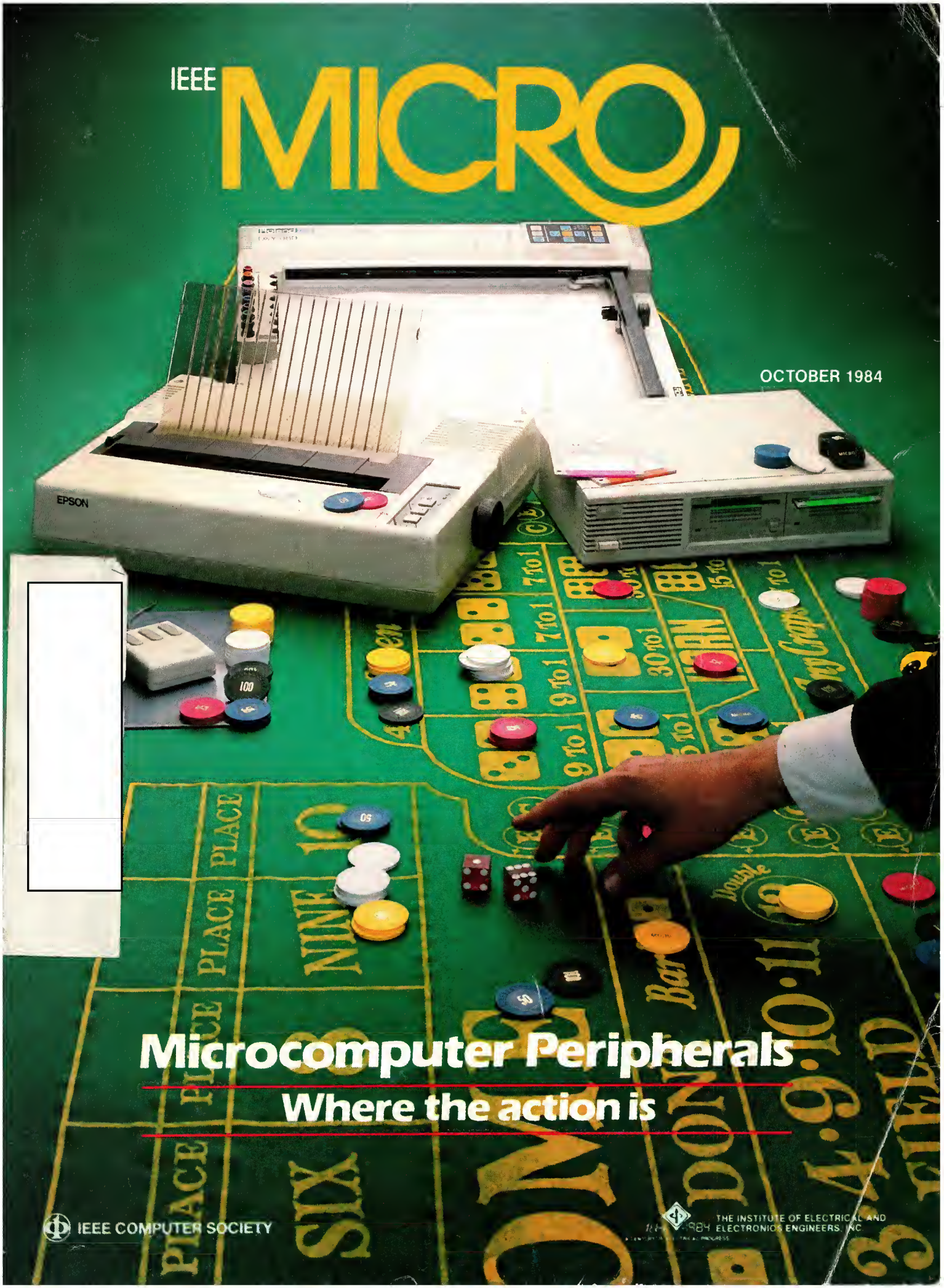
IEEE MICRO



OCTOBER 1984

Microcomputer Peripherals

Where the action is

IEEE COMPUTER SOCIETY

THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, INC

WE INVITE YOU TO JOIN US

IEEE COMPUTER SOCIETY

Membership Application

1884 · 1984 A CENTURY OF ELECTRICAL PROGRESS

Schedule of Fees (tax deductible)

IMPORTANT: Pay the FULL-YEAR rate if your application is postmarked between September 1, 1984 and February 28, 1985. Pay the HALF-YEAR rate if your application is postmarked between March 1, 1985 and August 31, 1985.

Membership expires December 31, 1985.

*IEEE members in Regions 7 (Canada) and 8 (Western Europe and the Mid-East) may deduct $6 from full-year rates, $3 from half-year rates. IEEE members in Regions 9 and 10 may deduct $13 from full-year rates, $6.50 from half-year rates. ACM members who join both the IEEE and the Computer Society may deduct $5 from full-year rates, $2.50 from half-year rates.

For applications received:	Half-Year 3/1/85–8/31/85	Full-Year 9/1/84–2/28/85
• **an IEEE member who wishes to join the Computer Society** ..... IEEE membership no._____	☐ **$5.00**	☐ **$10.00**
• **a non-IEEE member who wishes to join both IEEE and the Computer Society*** ..... Full IEEE members receive *Spectrum*, *The Institute*, and many additional benefits.	☐ **$52.50**	☐ **$90.00**
• **a non-IEEE member who wishes to join the Computer Society only**	☐ **$17.00**	☐ **$34.00**

Publication Options

If, in addition to your automatic subscription to *Computer* Magazine, you would also like to receive:

	add:	
• *IEEE Computer Graphics & Applications* (3061)	☐ $11.00	☐ $22.00
• *IEEE Micro* (3071)	☐ $7.50	☐ $15.00
• *IEEE Design & Test of Computers* (3111)	☐ $6.00	☐ $12.00
• *IEEE Software* (3121)	☐ $7.00	☐ $14.00
• *Transactions on Computers* (1161)	☐ $7.50	☐ $15.00
• *Transactions on Software Engineering* (1171)	☐ $8.00	☐ $16.00
• *Transactions on Pattern Analysis & Machine Intelligence* (1351)	☐ $6.00	☐ $12.00
• *Proceedings of the IEEE* (5011) (available only to IEEE members)	☐ $7.50	☐ $15.00

SPECIAL OFFER

Join now and receive a free book. Check one:

☐ *Microprocessors & Microcomputers*

or

☐ *Selected Reprints in Software*

Check box for additional information:
- ☐ Computer Society Membership Brochure
- ☐ Student Membership Application
- ☐ Publications Catalog

Total amount remitted with this application $_____

☐ Check or money order enclosed. (Make payable to IEEE. Mail to IEEE Computer Society, 10662 Los Vaqueros Circle, Los Alamitos, CA 90720.)

☐ VISA ☐ MasterCard ☐ American Express

Charge Card Number

Exp. Date Mo. Yr.

I hereby make application for IEEE Computer Society membership and, if elected, will be governed by IEEE's and the Society's Constitutions, Bylaws, and Statements of Policies and Procedures.

Full signature _____ Date _____

MAILING ADDRESS

First Name _____ Middle initial(s) _____ Last name _____

Street address _____

City _____ State/Country _____ Zip _____

EDUCATION (highest level completed)

Course _____ Degree received _____ Date _____

Name of educational institution _____ Date of birth _____ ☐ Male ☐ Female

OCCUPATION

Title or position _____

Firm name _____

Firm address _____

City _____ State/Country _____ Zip _____

Affiliate society membership no. (if applicable) _____ Grade _____

REFERENCE

(an IEEE member; if unknown, a managerial person who knows you professionally)

Name (print in full) _____

Position _____

Street address _____

City _____ State/Country _____ Zip _____

MAIL TO: IEEE COMPUTER SOCIETY, 10662 LOS VAQUEROS CIRCLE, LOS ALAMITOS, CA 90720.

IEEE MICRO

October 1984 Volume 4 Number 5 (ISSN 0272-1732)

THEME FEATURES

Cover: Microcomputer Peripherals—see "About the Cover," p. 6.

Design: Jay Simpson

DEPARTMENTS

Coming next issue:
Fault-tolerant microcomputing

Change of Address, p. 88
Reader Service Cards, p. 89

IEEE Micro

Editor-in-Chief: Peter R. Rony, VPI & SU*

Associate Editor-in-Chief:
J. Thomas Cain, University of Pittsburgh

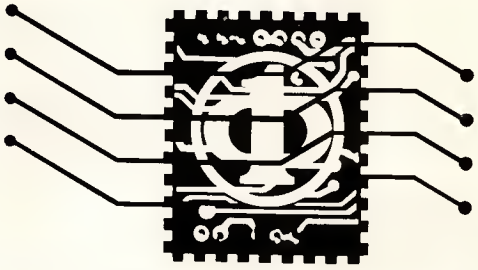
*Submit six copies of all articles and special issue proposals to Peter R. Rony, Dept. of Chemical Engineering, University of Delaware, Newark, DE 19716; (302) 368-5580.

Circulation: *IEEE Micro* (ISSN 0272-1732) is published bimonthly by the IEEE Computer Society, 10662 Los Vaqueros Circle, Los Alamitos, CA 90720; (714) 821-8380. Annual subscription: $12.00 in addition to IEEE Computer Society or any other IEEE society member dues. Nonmember prices: available on request. Single-copy prices: members $7.50; nonmembers $15.00. This journal is also available in microfiche form. IEEE Headquarters address: 345 East 47th Street, New York, NY 10017.

Undelivered copies: Send to 10662 Los Vaqueros Circle, Los Alamitos, CA 90720.

Postmaster: Send address changes to *IEEE Micro*, IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. Second class postage is paid at New York, NY, and at additional mailing offices.

LETTERS TO THE EDITOR



The MC68020—corrections and comparisons

Editor:

In the course of my work, I have found a few errors in the otherwise excellent article on the MC68020 by Doug MacGregor, Dave Mothersole, and Bill Moyer (August 1984, pp. 101-118).

Figure 15 shows a code fragment intended to manage two-level indexing. The code appears to be correct, but the lengths given are obviously wrong. If my hand assembly is correct, the length of the fragment in MC68000 code should be 13 words rather than 13 bytes, and the length of the fragment in MC68020 code should be 7 words (14 bytes) rather than 8 bytes.

Similar results for the NS32032 are

Code	11 bytes
Execution	25 cycles

from the code fragment

```
movzwd    class[r0:w], r1
cmpqw     0, count[r1:w]
beq       else:b
```

In this timing, the branch was not taken.

Jonathan Ryshpan
National Semiconductor

Author's reply:

I greatly appreciate Jonathan Ryshpan detecting the error in our article on the MC68020. In fact, Figure 15 should read "13 words" and "8 words" for the 68000 and 68020 code size, respectively.

I also appreciate National contributing the code sequence for the NS32032. I intentionally left reference to all other processors out of the article so that there would be no question about misrepresenting another company's microprocessor. Given this code sequence, however, I think that it would be very interesting to make such a comparison.

While the code sequence is close to the example that was given, there are several significant errors and omissions. In the code sequence for the NS32032 shown below, there are several problems:

```
                                        CODE SIZE
movzwd    class[r0:w],r1                (5 bytes)
cmpqw     0,count[r1:w]                 (4 bytes)
beq       else:b                        (2 bytes)
                                        (11 bytes)
```

First, the branch displacement size is word (not byte). I am willing to assume that it is less than 14 bits. Second, the class and count are treated as absolute addresses rather than as register-relative. In the 68020 example, the operand loaded into the register is addressed by base register + 16-bit displacement + scaled index. Third, the class and count are 16-bit displacements; if they are absolute addresses, then they must be considered 32 bits (which would expand the code size beyond that shown below).

Some minor adjustment must be made. The corrected NS32032 code sequence which is equivalent to the 68020 sequence is listed below, with the associated length in bytes:

```
                                        CODE SIZE
movzwd    class(r2)[r0:w],r1            (7 bytes)
cmpqw     0,count(r2)[r1:w]             (6 bytes)
beq       else:w                        (3 bytes)
                                        (16 bytes)
```

In this case, the code size of both the 68020 and the 32032 is the same.

When I reviewed the execution time of the code sequence provided by Ryshpan, I found his timings to be radically different from those provided in the *NS16000 Instruction Set Manual* of August 1983. This seemed like a reasonable reference, since there is no internal difference between the 32032 and the (then) 16000, and all operand accesses are 16-bit. The execution times I derived for the corrected code sequence are based on this reference. In addition, the assumption that the branch was not taken is wrong. The branch *was* taken in the 68020 timings. In the timings listed below, it is assumed that the operands are aligned, that there are three cycle accesses (no MMU), and that

cont'd on page 6

WHEN A PERSONAL COMPUTER ISN'T ENOUGH, YOU NEED A PERSONAL PDP-11.

NOW YOU CAN HAVE DIGITAL'S PERSONAL PDP-11'S RUNNING PDP-11 AND VAX-COMPATIBLE SOFTWARE ON YOUR DESK.

You know who you are. You've been doing a major part of your work using a terminal connected to a PDP-11™ or VAX™ system. Your applications are as wide-ranging as your knowledge. Theoretical physics, real-time data analysis, statistics, financial modeling, CAD/CAM, process control – there's very little that's beyond the reach of your professional experience.

Like most users, you're very satisfied with the services you've been getting from your PDP-11. You've come to rely on them, in fact. And you're not willing to give them up for just a personal computer. What you really want is a full-powered minicomputer dedicated exclusively to your work.

If you're this type of user, Digital has exactly the computers you need: the Professional™ 300 Series, our personal PDP-11's. They're engineered to give you the minicomputer power and sophistication you've come to expect – in a personal computer size, and at a personal computer price.

RICH PDP-11 DEVELOPMENT ENVIRONMENTS AT YOUR COMMAND.

Digital's Professional 300 Series, the best-engineered desktop systems for computer-experienced professionals, offer you a choice of minicomputer-powered operating systems.

First among these is P/OS,™ the Professional Operating System. A single-user, multi-tasking version of RSX-11M-PLUS,™ it gives you capabilities that far exceed typical personal computer software. Its complement of compiler languages includes BASIC 11, DIBOL, COBOL-81, Pascal, FORTRAN-77, and WHITESMITH C. What's more, a Native Tool Kit and a rich selection of editors, debuggers, task builders, forms management and sort utilities helps you achieve the high programming productivity you've come to expect from a minicomputer. The UCSD-p System™ is available as an alternative development environment under P/OS. Plus, P/OS lets you use Digital Classified Software, a portfolio of proven applications such as TK! Solver,™ a high-performance equation-solving tool, and RS/1,™ an industry-standard laboratory research system.

Next, there's PRO/RT-11,™ a single-user, multi-tasking, real-time version of the RT-11 operating system that's so popular in technical OEM PDP-11 applications. There's also the STANDARD MICRO MUMPS 300™ System. And for commercial applications there's the CTS 300™ system, which features RT-11 DIBOL portability.

VENIX,® a UNIX® V7M operating system complete with Berkeley 4.1 enhancements, has been optimized for the Professional Series. It even includes a UNIX System 5 software license, demonstrating our commitment to keeping the Professional current with future UNIX directions.

MINICOMPUTER STRENGTH APPLICATIONS. ON THE SHELF. READY TO GO.

The reason we've engineered the Professional with a variety of operating systems isn't just to let you write your own minicomputer-powered programs. It's to let you access a vast library of proven, developed PDP-11 and VAX programs, and run them independently on your Professional.

Many third-party PDP-11 and VAX applications – or the ones you're using now – can be transported to your Professional. You can use the same files, the same commands. This puts an incredible variety of scientific, industrial, technical and commercial solutions at your disposal.

Just as important, you can attach a real-time interface to the Professional to adapt it for scientific and industrial use. And you'll have a wide variety

of printers, plotters, and special purpose peripherals to choose from.

A TRUE DISTRIBUTED OFFICE WORKSTATION ON YOUR DESK.

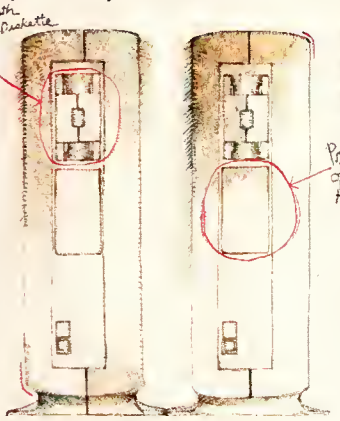
The Professionals acknowledge the fact that you work in an office as well as in a lab, offering Pro Office Workstation, the Professionals' version of Digital's ALL-IN-1™ software, the best-engineered office automation system you can buy. Running in conjunction with a VAX host, ALL-IN-1 gives you word processing, automatic spelling verification, electronic filing, electronic mail, calendar management and more. And that can increase productivity organization-wide.

Office automation tools designed for independent use on your Professional include Digital's ASKIT™ software, which provides business graphics, personal database, word processing and spreadsheet functions, plus a game. And with the optional CP/M® Softcard, you can run a variety of CP/M-80 packages on your Professional.

ETHERNET/DECNET LOCAL AREA NETWORKING TODAY.

The Professional 300 Series supports a variety of networking options. Foremost among these options is DECnet,™ which lets your Professional serve as a distributed workstation with PDP-11 and VAX processors. And, DECnet gives you a choice of local and wide-area communications devices, including 10 Mb/sec Ethernet, with full support for V2.0 standard (IEEE 802.3 specification); public packet-switched X.25 networks; and standard telephone lines.

And by virtue of its compatibility with PDP-11 and VAX software and RMS file structures, the Professional lets you download remote files from your PDP-11 or VAX to your Professional, all transparently to the user and the program. Or, if you wish, your Professional can emulate Digital's VT™ terminals.



The Professional doesn't leave out the rest of the world, either. Device emulation includes IBM 3270, 2780/3780, 3277, and more.

THE LEADING GRAPHICS WORKSTATION IN ITS CLASS.

If you only want to portray simple X-Y values, lots of personal computers can do the job. But if you need a way to graphically display thousands of information variables, there's no finer tool available than a Professional. It gives you a palette of 4,096 colors to work with. State-of-the-art graphics architecture, like GIDIS,™ a virtual device interface, helps you design fast graphics for your programs, while allowing them to run independently of future hardware enhancements. Industry-standard graphics application interfaces are also available. And the Virtual Device Meta file capability lets you integrate text and graphics in a single file under P/OS 2.0. Just as important, the quality of Professional 300 graphics is unsurpassed. The bit mapped screen provides a 960 x 240 pixel resolution. And Digital's IVIS™ Interactive Video System is available for advanced program development.

BEST ENGINEERED MEANS ENGINEERED TO A PLAN.

The Professional 300 Series, like every Digital hardware and software product, is engineered to conform to an overall product plan. This means Digital systems are engineered to work together easily and expand inexpensively. Only Digital provides you with a single, integrated computing strategy from desk top to data center.

For more information on Digital's Professional 300 Series systems, the Professional 325 and the Professional 350, call 1-800-DIGITAL, ext. 690. Or send the coupon or write: Digital Equipment Corporation, Attn: Mr. Dennis Coady, 200 Baker Avenue, West Concord, Massachusetts 01742.

I'd like more information on Digital's Professional 300 Series, the Personal PDP-11's:

☐ Please send a copy of your new Professional Series Handbook.

☐ Please have a sales professional call with complete information.

Name

Title

Company

Address

City

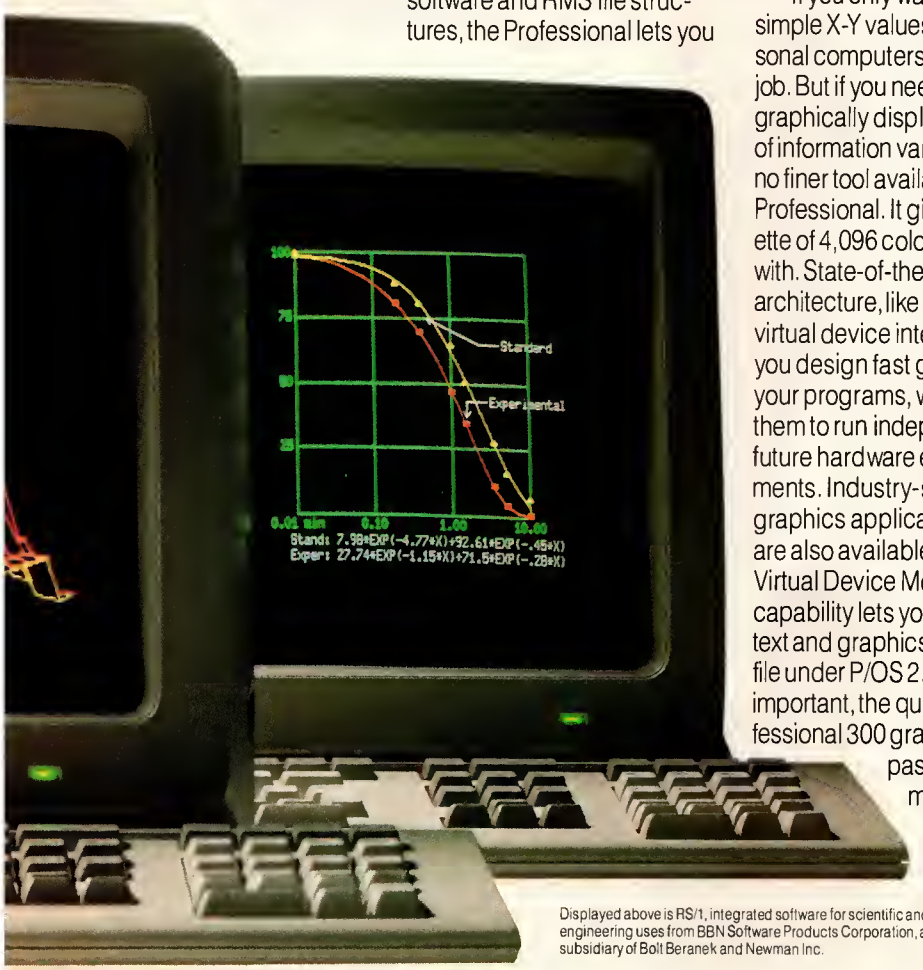
State Zip

Telephone Ext.

Return to: Digital Equipment Corporation, Attn: Mr. Dennis Coady, 200 Baker Avenue, West Concord, MA 01742. Media Code: N.

THE BEST ENGINEERED COMPUTERS IN THE WORLD

digital™



Displayed above is RS/1, integrated software for scientific and engineering uses from BBN Software Products Corporation, a subsidiary of Bolt Beranek and Newman Inc.

Reader Service Number 25

Letters *cont'd from page 3*

for every option, the execution time is minimum:

		CLOCKS	
movzwd	class(r2)[r0:w],r1	20	
cmpqw	0,count(r2)[r1:w]	15	
beq	else:w (taken)	16	
		51	clocks

If there are any errors in this accounting, I would like to know about them, but my source is the National manual.

While reviewing this case, I noticed that I had poorly annotated the conditions under which the timings were measured. In order to fairly compare the 68020 to the 68000, the cache was disabled. When the cache is enabled, the timing is different.

All this invites a performance comparison, of course. Using these timings, I have compared the execution times on a 12.5-MHz 68000, a 10-MHz 32032, and a 16-MHz 68020:

			CLOCKS	TIME
68000 @ 12.5 MHz			79	6.3 μs
32032 @ 10 MHz			51	5.1 μs
68020 @ 16 MHz	no cache	(68000 code)	50	3.1 μs
68020 @ 16 MHz	cache	(68000 code)	42	2.6 μs
68020 @ 16 MHz	no cache	(68020 code)	32	2.0 μs
68020 @ 16 MHz	cache	(68020 code)	24	1.5 μs

I thank Mr. Ryshpan for finding the error as well as for providing the code sequence upon which a comparison could be made.

Doug MacGregor
Motorola, Inc.

ABOUT THE COVER

Microcomputer peripherals . . . where the action is

There *is* much action in the world of microcomputer peripherals today, with rapid technical progress being made in every area from ink-jet printers to sub-5.25-inch hard disks to input peripherals such as mice. But is that progress rapid enough to keep pace with the stunning developments in microprocessor technology? Among peripherals, are there advances just as eyebrow-raising as a 450,000-device single-chip CPU? The answer is that there are, though they don't seem to garner quite the attention that the chips do. Yet consider the technique underlying ink-jet printing . . . or optical disks. Think about the cleverness of innovations like vertical encoding on magnetic media. And what about those Winchester heads literally *flying* at some outrageously low altitude over the surfaces of metal platters?

We are fortunate, too, that these advances are being made at the pace they are. As author Andrew Allison points out in his article (see page 9), the innovations have been coming just fast enough to keep up with the developments in the microchip world. Microprocessor-based computers and their peripherals are marching forward in step with one another, to the benefit of the user.

Our cover shows some representatives of the state of the art. We show an input peripheral, two output peripherals—one for text (well, *mostly* for text) and one for pictures, and a mass storage device. All four are commercially available; all four are small, light, and extremely capable.

Our mouse is an optical device manufactured by Mouse Systems of Santa Clara, California. Designated the PC Mouse, it is designed for use with the IBM Personal Computer. It comes with customized pop-up menu software for use with popular programs like Lotus 1-2-3, Visicalc, Multiplan, Volkswriter, and Wordstar. To eliminate moving parts (and the need to clean them), Mouse Systems used an LED reflecting off a special pad to a sensor to register motion, instead of the more conventional rolling ball. The PC Mouse retails for $195.

Our printer is one of many offered by Epson—in this case, an FX-80, one of the new breed of low-cost, high-performance dot-matrix microcomputer printers. Unavailable for our photo session (at the time, it was newly introduced and in short supply) was the LQ-1500, a state-of-the-art dot-matrix printer with a 24-pin printhead, a 200-character-per-second maximum speed, and three printing modes—draft, letter quality, and graphics. The LQ-1500 offers this capability for $1395.

Our plotter is Roland DG's DXY-880, an eight-pen unit featuring HP Graphics Language emulation. The Los Angeles-based company has designed the DXY-880 to sit on a table at a 60-degree angle so that it will occupy a minimum of space. The plotter features a serial (RS-232) and a parallel (Centronics) interface, a 3K buffer, 24K ROM, 0.05-mm resolution, and 200-mm-per-second speed. It sells for $1295.

Our mass storage unit is a dual-disk drive from Hewlett-Packard featuring 3.5-inch, hard-jacketed floppy technology. Each drive mechanism in the HP 9122D can format double-sided disk media to store 630K to 788K bytes, depending on the computer system and programming language used. This memory system is one in a family of HP 3.5-inch drives.

For further information on these products, circle the reader service number on the card at the back of the magazine—60 for the PC Mouse, 61 for the Epson LQ-1500, 62 for the Roland DG Model DXY-880, and 63 for the HP 9122D.

GUEST EDITOR'S INTRODUCTION

Advances in Microcomputer Peripherals

Jean-Daniel Nicoud
Swiss Federal Institute of Technology, Lausanne

Not too many years ago, computer peripherals were huge and expensive. Today's microcomputer peripherals, however, are small and efficient, and they provide better performance at much lower cost than their counterparts of 10 years ago. The evolution of microcomputer peripherals is far from over, though. The progress being made in magnetic media, flat screen displays, laser printers, sensors, local networks, input devices, and VLSI interface and controller chips shows that the most dramatic developments are yet to come.

Technology influences applications. The tasks to which computers are applied reflect the capabilities provided by a particular level of technology. The evolution of computers is toward artificial intelligence, i.e., the selection of an appropriate response to a complex problem. Just storing the information associated with such a problem is a challenge now, in terms of both memory size and methods of inputting the information.

As applications track technical evolution, we find (and will find) computers being used for a continually expanding range of tasks:

- by 1950, for number crunching, data processing, and communication,
- by 1984, for text processing, drafting, and information archiving, and
- by 2000, for AI-based simulation, design, and education.

The progress made in the first stage depended primarily on increases in processor power. The same will be true for the last stage. The intermediate stage of computer applications—where we find ourselves today—has been and will continue to be strongly influenced by the technology of peripherals:

- Text processing will reach maturity soon as a result of the progress in laser and ink-jet printing.
- Drafting systems, popularly called computer-aided design systems but still far from real integrated design tools, are nonetheless being improved with better input and output devices.
- Archiving large amounts of information electronically will become more effective than archiving such information on paper, due to advances in mass storage device technology.

The peripherals needed to support these applications are

0272-1732/84/1000-0007$01.00

Proceedings of the conference

The full proceedings of the International Conference on Advances in Microcomputer Peripherals can be obtained from Presses Polytechniques Romandes, EPFL—Ecublens, Centre Midi, CH-1015 Lausanne, Switzerland. The proceedings include approximately 20 papers; the price is SFr. 60.00 plus postage. A full description is available from the publisher.

easy to name: printers, plotters, displays, mice, tablets, scanners, and disks.

The evolution of peripherals affects the evolution of other products. For example, portable personal computers, the development of which is now exploding, have benefited from the availability of small printing mechanisms, small displays, and small mass storage devices. More data will be prepared and handled with such computers, but the development of mainstream desktop machines—with greater and greater peripheral and processor performance—will also continue.

To assess the status of and trends in microcomputer peripheral technology, the Swiss Federal Institute of Technology—Lausanne organized the International Conference on Advances in Microcomputer Peripherals, held October 9 through 11, 1984. The articles appearing in this special issue of *IEEE Micro* are adapted from papers presented at that meeting. It is difficult to cover all the interesting developments in microcomputer peripherals at a small international conference. It is even more difficult to do it in a special issue that features only a selection of the conference papers. Those which we did select either examine general aspects or describe particular techniques.

"Microcomputer Peripherals—Status and Trends," by engineer and market analyst Andrew Allison, surveys existing devices and technologies and discusses future developments. In "The Non-Death of Paper," Roy G. Lahr, a well-known consultant in the area of printer technology, predicts the healthy survival of paper despite the announcements, for years now, of the paperless society.

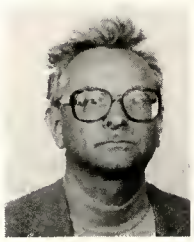
In the area of technique, Peter D. Noakes and Robert Aish ("A New Peripheral for Three-Dimensional Computer Input") present the results of an original research project aimed at the problem of entering spatial information into a computer. Wolfgang Doster and Richard Oed ("Word Processing with On-Line Script Recognition") describe their work on a more widely acknowledged but no less important problem: computer recognition of handwritten information.

Analog VLSI circuits open the door to new applications. Ernst Habekotté and Stefan Cserveny, in "A Smart Circuit for a Capacitive Microtransducer," discuss a CMOS switched-capacitor A/D converter for a capacitive microtransducer. This converter and transducer comprise a two-chip solution to the problem of analog data capture.

Because most peripherals now embody at least one microprocessor to provide some degree of "smartness," advances in microprocessor technology are of high interest to designers of peripheral equipment. The availability of low-power CMOS microprocessors, for example, has made it possible to design units powered by small battery packs. And the development of more compact types of microprocessor packages has further contributed to the physical shrinking of peripheral devices. Jim Farrell, in "The Advancing Technology of Motorola's Microprocessors and Microcomputers," shows what one manufacturer can do.

Our articles do not constitute anything like a complete survey of peripheral technology, of course. We must at least mention special-purpose VLSI circuits, which promise to reduce further the size and cost of peripheral equipment by integrating more and more functions on smaller and smaller amounts of silicon. Software in all its aspects is also missing from our coverage. Software is now a part of functions that have always been regarded as involving hardware only—it is playing a larger and larger role in enabling designers to maximize the performance and usability of mechanical and electronic features.

Although our treatment is incomplete, our authors have nonetheless addressed many important issues in the few pages available to them. We thank them, and the reviewers, for their efforts. ■



Jean-Daniel Nicoud is a professor at the Swiss Federal Institute of Technology in Lausanne, Switzerland. He has been active in microprocessor-related research for more than a decade and has designed many microprocessor-based systems. His and his research group's interests include microcomputer design, development tools, local networks, microcomputer peripherals, graphic workstations, laser printers, and computer-aided design.

Nicoud received a degree in engineering physics from the Swiss Federal Institute of Technology in Lausanne, and a PhD degree in electrical engineering from the same institution in 1969. He has been an associate editor of *IEEE Micro* since its inception.

Nicoud's address is École Polytechnique Fédérale de Lausanne—Laboratoire de Microinformatique (EPFL—LAMI), 16 Chemin de Bellerive, CH-1007 Lausanne, Switzerland; telephone (021) 47 26 42.

The mass storage and input/output needs of microcomputer systems are driving the development of a broad range of peripheral products. Fortunately, no one technology is lagging—the capabilities of all peripherals are advancing at compatible rates.

Microcomputer Peripherals

Status and Trends

Andrew Allison

The growth in microcomputer utilization has depended, in large measure, upon the availability of appropriate peripheral support—particularly mass storage. "Appropriate," in this context, means products that offer performance that meets typical application requirements at prices compatible with those of the processor and main memory components. Fortunately, the pace of developments in peripheral equipment technology appears to be about the same as that in the semiconductor field, and the rapid growth of the microcomputer market is resulting in broadly similar price/performance trends. This review of the status of and design trends in peripheral technology encompasses conventional data storage, input and output devices, and the typically board-level products employed for communications and specialized I/O. It excludes coprocessors and specialized board-level processors.

Electromechanical storage devices form a hierarchy based upon access time, and they are reviewed here in that context. It must be remembered, however, that the highest-speed class of products, hard disks, has an absolute dependence upon backup via some form of removable medium. Only the cartridge disk approach to backup is considered in the hard disk section of this article, while the floppy disk and magnetic tape alternatives are reviewed under those categories of peripheral. Bubble memory is a special case, but is included in the mass storage section for convenience.

Terminals are subdivided into alphanumeric and graphic categories on the basis of their quite different requirements and probable evolutionary paths, as are printers. (Fully formed character and dot-matrix printers are regarded as analogous to alphanumeric and graphic displays.) Plotters are included with printers on the basis of the similarity of their functions, as are local network products with the more general communications interfaces. Two other classes are I/O device are reviewed here—voice, and measurement and control (i.e., analog, and direct digital I/O).

Mass storage peripherals

As indicated above, mass storage peripherals form a hierarchy based on access time. This hierarchy should be viewed as part of an overall memory systems hierarchy (see Figure 1); here, however, only the secondary and backup/archival storage portions are reviewed.

Despite efforts to develop alternative mass storage mechanisms such as optical disks, magnetic media are ex-

0272-1732/84/1000-0009$01.00 © 1984 IEEE

pected to remain the preferred choice throughout the 1980's. The key trends in microcomputer mass storage design are the rapid growth in the use of Winchester disk drives, the integration of their controllers, and ever-increasing capacity. Single-chip controllers are becoming available for the very high volume 5¼-inch products and, once standards have evolved, will quickly follow for sub-5¼-inch drives. The two significant trend in controller design is a movement towards integrating the common elements of hard disk, floppy disk, and magnetic tape backup controllers, which will result in compact, low-cost, frequently single-board system implementations.

The long-term trend in magnetic media capacity is almost the same as that for semiconductor memory—it doubles every two to three years. As with semiconductor memory, this trend is confidently expected to continue for at least the next several years. One way that this is being achieved is through increases in track density. In the case of hard disks, the popular open-loop, stepper-motor designs supporting about 400 tracks per inch (160 tracks per cm) are giving way to closed-loop, voice-coil implementations. The latter provide track-following capability by incorporating servo information into the data tracks and linear movement. This, in turn, permits density to be increased to the 1000-track-per-inch (400-track-per-cm) level. Closed-loop control is also entering the floppy disk field, resulting in a doubling of the present 96-track-per-inch standard. In the case of magnetic tape, standard ½-inch drives are moving from the present 9-track to the 19-track level. Another approach to increasing hard disk capacities has been to increase the number of platters. Maxtor Corporation of Santa Clara, California, for example, offered the first eight-platter, 960-track-per-inch, 5¼-inch units, with capacities of up to 380 megabytes per drive, in 1983.

The other major thrust in the search for higher capacity is that towards increased bit density, which has been doubling every three years for the past twenty (Figure 2). Future increases will come from changes in materials technology, which is moving away from the traditional ferric oxide dispersed in a binder. On the one hand, sputtering techniques, which place a film of pure ferric oxide on the platter, are being refined. This provides greater flux, and hence recording, density. Similar increases in capacity are being made available through the use of plated media, which began to enter limited production in 1983. Either technique appears capable of raising density from the 12,000-bit-per-inch (5000-bit-per-cm) level currently achievable with oxide-in-binder media to about 60,000 bits per inch (25,000 bits per cm). Flexible media, both disk and tape, will continue to offer maximum bit densities of about half those achievable for hard disks.

New recording and playback techniques will increase capacity by at least another factor of five during the next few years. This will come primarily from the switch to vertical, rather than horizontal, recording techniques. The former orient the magnetic fields representing data side by side rather than end to end, permitting greater densities. Japanese suppliers, many of whom are devoting considerable resources to vertical recording, have demonstrated 300,000-bit-per-inch (120,000-bit-per-cm) density. The following sections review the impact of these broad technological trends on the individual storage mechanisms.

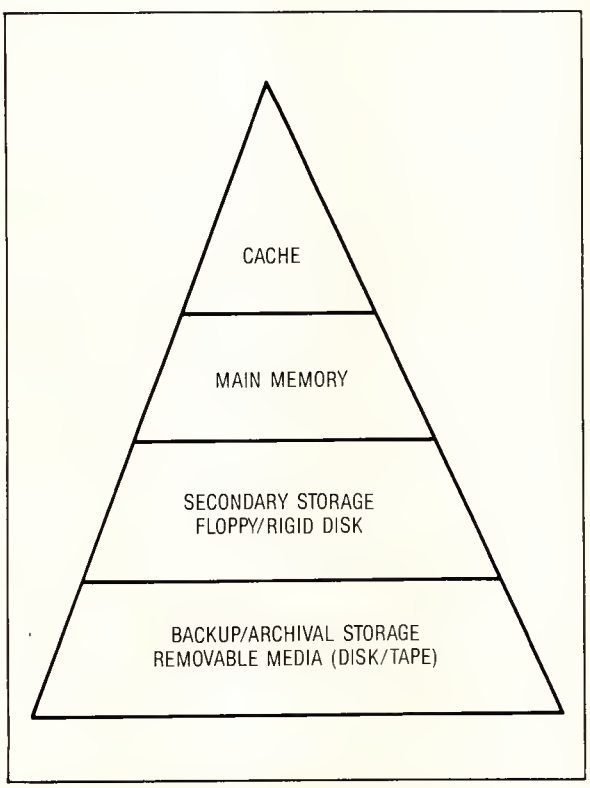


Figure 1. The memory subsystems hierarchy.

Hard disks. In 1983 the small-computer hard-disk storage market was dominated by 5¼-inch Winchester drives with 5 to 10 megabytes of formatted storage capacity. The de facto standard interface was the Seagate ST506, and Seagate's line of one-, two-, and three-platter (5-, 10-, and 15-megabyte) drives accounted for almost half the total 5¼-inch unit sales. During the same year, half-height drives were shipped by every major manufacturer, and these units appear likely to predominate in low-end microcomputer configurations by 1985. Due to the large market, the frenetic competition between the (temporarily) large number of suppliers, and IBM's choice for the PC/XT, 10-megabyte, 5¼-inch Winchester disk drives were selling for well under $400 in high volume during the first half of 1984, and can be expected to break the $250 barrier in 1985. Meanwhile, 20-megabyte, half-height drives will be available from a number of sources by year's end.

During 1983, the steady advance in bit density began to put serious pressure on the ST506 standard, with its 8K-byte-per-track and 5-megabit-per-second transfer-rate limitations. The former makes increases in bit density irrelevant (for a given size of disk), while the latter constrains the maximum bit density that can be supported at the standard rotational speed of 3600 rpm. As a result, the upper limit of ST506-compatible capacity is 12 to 15 megabytes (formatted) per platter, little more than the current standard 10-megabyte capacity. In response to this pressure, new interface standards were proposed by

three different groups of manufacturers in 1983. One group, led by Maxtor, proposed the ESDI, the Enhanced Small Disk Interface, with a 10-megabit-per-second transfer rate. This proposal retains the ST506 cable and connector, but little else. Another group, led by Xebec of Sunnyvale, California, promoted the 10-megabit-per-second ANSI interface standard originally developed for 8-inch drives. Both groups consisted of small makers of high-performance drives hoping to take the initiative from market leader Seagate, but Xebec subsequently abandoned the ANSI standard in favor of ESDI.

Meanwhile, in September 1983 Seagate announced its own high-performance standard—and the support of number two supplier Tandon. By providing an initial maximum transfer rate of 10 megabits per second and the possibility of a further increase to 15 megabits per second, but otherwise retaining compatibility with the ST506 standard, the Seagate ST412-HP interface seems likely to become the preferred choice for low-cost, high-performance drives with capacities of up to about 80 megabytes. The ESDI approach, with data separation performed at the drive rather than within the controller, offers advantages for 100- to 400-megabyte drives.

The need still remains for a very-high-performance interface. Average access times are decreasing from the 83 milliseconds typical of 1983 low-end products to the 35-millisecond range, and bit densities continue to increase. The leading candidates for a very-high-performance standard appear to be the multilayer Intelligent Peripheral Interface under development by ANSI X3T9.3 and an enhanced version of the SMD standard originally developed for 14-inch drives and already at 16 megabits per second.

The capacity of high-performance, 5¼-inch Winchester disk drives is expected to rise in parallel with the increasing mass storage requirements of high-performance microcomputer systems. Thus, it appears likely that such drives will remain the secondary storage medium of choice for some time to come. Meanwhile, the sub-5¼-inch drive is expected to begin to penetrate low-end microcomputer markets. Although an extremely attractive physical configuration, the micro-Winchester drive has suffered from a proliferation of proposed media specifications. By mid-1984 it began to appear that this was being resolved in favor of the 3½-inch configuration.

The physical attributes of the micro-Winchester drives imply that they will offer approximately half the maximum capacity of their mini-Winchester (5¼-inch) cohorts at any given level of hard disk technology development. Alternatively, if historic capacity trends are maintained, micro-Winchester capacity can be expected to lag that of mini-Winchesters by about two and one-half years. Based on this, it seems reasonable to assume that sub-5¼-inch drives with capacities in the 10- to 20-megabyte range will predominate in the low-end microcomputer markets by the end of 1986, probably in conjunction with an integrated microfloppy disk or, less likely, cassette-tape backup and controller. The availability of highly integrated ST506 controllers will encourage the use of that interface for the sub-5¼-inch drives, at least until higher-performance integrated controllers are developed.

For 8-inch drives, maximum capacity will remain approximately double that of 5¼-inch drives, and this configuration will satisfy the requirements of minicomputer and low-end superminicomputer applications. The 14-inch drive, which offers a further doubling in maximum capacity, will be used only for the relatively few small-computer applications having very large storage requirements—in addition, of course, to its traditional role in mainframe mass storage.

A few suppliers are working on cartridge disk drives, typically removable cartridges having the same capacity as single fixed platters. There have been considerable difficulties in getting such drives into production and several companies have dropped out, but some 10/10 (10 megabytes fixed and 10 megabytes removable storage) drives are available. The trend towards closed-loop control already evident in fixed-disk products is of benefit to cartridge proponents since it makes possible interchangeability—a prerequisite for this type of storage.

Assuming that reliability proves adequate and media cost and availability problems can be resolved, the fixed/removable disk configuration could provide a convenient, high-performance, transaction- or file-oriented backup and program loading mechanism. However, the relatively high cost and limited capacity of the media make the fixed/removable drive unsuitable for archival storage, and it may be overtaken by floppy-disk and cassette-tape alternatives. If removable rigid disks do become widely used, the ultimate mass storage subsystem of choice may turn out to be a fixed/removable disk configuration backed up by a cartridge-tape drive. In the meantime, floppy disks will continue to play an important role.

Floppy disks. As in the case of hard disks, the floppy-disk market is dominated by 5¼-inch products. Other similarities are the overwhelming market share of a single

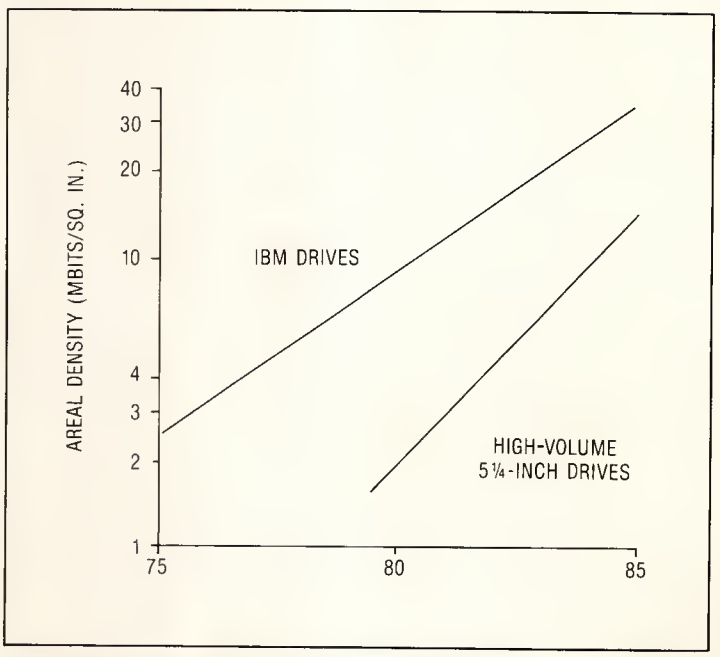


Figure 2. Winchester disk areal density vs. time.

supplier and the frenetic competition for the rest of the market. The floppy-disk market is ahead of that for hard disks in the race for commodity status and Tandon, as a fully integrated supplier with about one-third of the total market, has been setting a stiff pace—its 1983 sales doubled for the fifth consecutive year, reaching $300 million. However, price leadership appears likely to be taken over by Japanese suppliers, who have brought tremendous half-height, double-sided/double-density capacity (250,000 units per month from one supplier alone) on line during 1984.

In 1983, the mainstream double-sided, double-density (96-track-per-inch, 40-track-per-surface) drives providing a half-megabyte of capacity were offered in half-height configurations by many manufacturers. High-capacity drives utilized up to 160 tracks, at track densities of 192 tracks per inch, and high bit density to store as much as 3.33 megabytes. As with hard disks, these capacities can be expected to double every two and one-half years, and maximum capacities approximately double with each step in the sub-5¼-inch, 5¼-inch, and 8-inch media size series. Sub-5¼-inch media have had the same media proliferation problem as their hard disk counterparts, with 3-, 3¼-, and 3½-inch standards being proposed; however, it seems fairly certain that the 3½-inch version will predominate.

The media proposals fall into two categories, hard- and soft-jacketed. Hard-jacketed diskettes are surrounded by a plastic case with a shutter on the read/write window to protect the medium from contamination when outside the drive. Sony Corporation, Shugart Associates, and Tandon are producing drives utilizing a 3½-inch, hard-jacketed diskette, and a consortium of Japanese suppliers led by Hitachi is promoting a 3-inch version.

Of the two hard-jacketed proposals, the 3-inch Japanese version offers capacity and interface compatibility with 5¼-inch drives in the smallest package (1.57 × 3.54 × 5.9 inches). However, the slightly larger diskette for the 3½-inch drive allows easier (i.e., lower-cost) implementation of a given capacity. The physical compatibility with the micro-Winchester drive (for which the microfloppy is the natural backup mechanism) being promoted by the 3½- and 3¼-inch proponents is also an advantage. The confusion engendered by the multiple media sizes has delayed full development of the sub-5¼-inch floppy market. However, the 3½-inch hard-jacketed products are clearly predominating.

Minifloppy (5¼-inch) disks remain the leading backup for 5¼-inch Winchester disks and, due to their convenience and low cost, will remain part of most system configurations indefinitely. By 1985, however, fixed/removable drives and/or cassette-tape drives are expected to begin to take over the archival storage function for 8-inch and 5¼-inch Winchester drives.

The 8-inch floppy disk has a somewhat tenuous future. Mini- and microfloppies offer enough storage for most floppy-only mass storage subsystems, and they provide backup for hard disks of the same sizes as well. Standard 8-inch Winchester disks are expected to be used only in high-performance systems where the (currently) higher cost of magnetic-tape backup, whether cassette or conventional reel-to-reel, can be readily justified. Thus, it appears likely that the use of 8-inch floppy disks will decline.

Backup/archival storage. Magnetic tape, in its half-inch, reel-to-reel implementation, is the standard backup medium for very large amounts of data. Although magnetic-tape backup is intrinsically attractive for mini- and micro-Winchester disks, a combination of cost and physical size constraints has prevented its widespread adoption. This is in the process of changing, under the influence of several forces. The proliferation of small hard disks and their rapidly increasing capacity are severely straining the backup capability heretofore provided by floppy disks. At the same time, the adoption of standards such as the QIC-02 controller-to-drive interface and the QIC-24 data format for the quarter-inch cartridge streaming tape drive is providing the multiple sourcing and media interchangeability required for removable media (although standards compatible with those employed by floppy or hard disks would be more acceptable). Finally, cassette-tape drives in the half-height, 5¼-inch form factor are becoming available, matching the trend in hard-disk design.

The only remaining barrier to widespread utilization of quarter-inch streaming tape drives is their relatively high cost, and multiple sourcing and the large potential market should take care of that. Assuming that this occurs, the quarter-inch tape and removable-disk cartridge will battle it out for dominance of the mini-Winchester backup market, with tape probably having the edge. As indicated above, tape capacity is increasing at essentially the same rate as hard-disk capacity, and it is anticipated that the capacity of the already standard quarter-inch cartridge will keep up with that of 5¼-inch hard disks. Half-inch tape cassettes are also being promoted as a backup medium for 5¼-inch Winchester drives but, despite the introduction of a product by Tandon and a rumored joint effort by Tandon, Seagate, and DEC, this is unlikely to succeed unless it too can be packaged in the half-height configuration.

The 8-inch Winchester drive presents something of a problem in that the smaller market anticipated for these products will inhibit the development of backup products specifically designed for it. The most likely outcome is for the ¼-inch streaming tape drives developed for 5¼-inch, or the ½-inch tape drives developed for 14-inch, Winchester disk backup to be employed within 8-inch systems. A possible alternative would be an integrated disk and (probably half-inch) tape subsystem. It should be kept in mind that there is no reason why a fixed hard disk should occupy front panel space.

The order-of-magnitude difference in storage capacity between hard and floppy disks and the limits to transport speed of magnetic-tape backup call for file- or transaction-oriented backup rather than the dumping of the entire disk. Techniques to facilitate this kind of backup are evolving, particularly in the fast-growing on-line transaction processing application area, and will (we hope) find their way into the standard operating systems. The need is for semiautomatic saving of files and data in a form that makes it feasible to easily restore the system in the event of a disk crash.

Bubble memory. Ever since its development at Bell Labs in 1967, bubble memory has been a disappointment to its more ardent proponents. As a block-structured, solid-state memory technology, it has offered the promise of replacing rotating mass memory in rugged electrical and mechanical environments. Unfortunately, the complexity of its interface requirements and the failure of suppliers to support it with highly integrated controllers and interface circuits have resulted in poor acceptance. The continuing pace of development for rotating memory products seems likely to inhibit the widespread utilization of bubble memory storage.

The most probable general-purpose market for bubble memory—portable personal computers—is already served by the 5¼-inch and sub-5¼-inch rotating memory products reviewed above; in order to compete, a bubble memory subsystem would have to occupy the same volume, cost about the same, and provide 5 to 10 megabytes of capacity. With half-height, double-sided, double-density floppy disks selling for $75 and 10-megabyte hard disks approaching $300 in mid-1984, this represents quite a challenge. (Any cost comparison must take into account the lower power requirements of bubble memory, of course.) Bubble memory design and manufacturing have much in common with standard semiconductor memory, and densities can be expected to increase from the 4 megabits per chip currently available at the same rate as the other storage media discussed here. However, absent a significant penetration of the portable computer market, bubble memory will remain largely a niche technology.

Absent a significant penetration of the portable computer market, bubble memory will remain largely a niche technology.

Video display terminals

The review of display terminal design trends that follows is limited to terminals utilized with general-purpose small-computer systems. In the case of alphanumeric terminals, this restricts the field to matrix-display editing terminals and excludes dumb, intelligent, and computer-specific data entry terminals (e.g., the 3270 and VT100 and their many emulations).

Little change is expected in the bread-and-butter editing display terminal product, as manufacturers continue to seek reduced manufacturing costs in this extremely competitive market. The standard 12-inch, 80-character, 24- or 25-line display with a detached keyboard is evolving to comply with the DIN ergonomic requirements that are rapidly becoming worldwide standards. The major trends in editing terminal design are increasing functionality at the low end, availability of full-blown personal computer capability at the low end, and a shift to flat panel displays. The demand for compact displays engendered by the rapid growth of the portable personal computer market is accelerating the development of full-sized—i.e., 80-character by 24-line—flat panel displays, and such products are likely to become cost-effective for the high-volume, general-purpose market in the 1985/86 time frame.

Moving up in capability, low-cost, high-resolution 14- or 15-inch terminals with full-page (80-character by 66-line and 132-character by 24-line) display capability are beginning to penetrate the mass market. Such displays are expected to become standard within mid-range and high-end personal computer systems by 1987, as they already are in the CAD/CAE workstation market. The late-1983 introduction by HP of a microcomputer system that incorporates a touch-sensitive screen is anticipated to create additional interest in this alternative to the "mouse" approach to screen-coordinate addressing. However, the rapid and broad acceptance of detached keyboards and truly portable PCs militates against the long-term popularity of either touch screen or mouse since, with the keyboard on one's lap, one can reach neither the screen nor a surface for a mouse. Aside from the extremely cost-sensitive editing terminal, the key display product during the next few years appears likely to be the editing terminal with graphics capability. The demand for this product, which has arisen in response to the proliferation of micro- and microminicomputer systems, is expected to grow very rapidly. Bit-mapped, raster-scan terminals are already achieving significant penetration in the small systems market, with color capability not far behind, and are expected to predominate in every area but the very low end of the editing terminal market by 1986. As with the standard alphanumeric terminal, the fundamental design objective will be to achieve low manufacturing cost—little technological innovation is anticipated in the products themselves.

The most significant trend in the display area is that towards graphics software standards. Although primarily oriented towards the high-performance graphics terminals discussed below, graphics standards such as the GKS (Graphical Kernel System), developed in West Germany but already being considered for adoption by ANSI, will spread quickly in the low-end market. This trend is likely to be accelerated by the development of VLSI controllers that will incorporate standard features. Some 15 US suppliers have also announced their support for the NAPLPS (North American Presentation-Level Protocol Syntax) standard for the transmission of text and graphics information, and for the CGI (Computer Graphics Interface) standard to provide a common set of functions not just for any display terminal, but also for as many other graphics display devices (pen plotters, etc.) as possible.

At the high end, the explosive growth in CAD/CAE applications being brought about by the microcomputer is fueling demand for low-cost, high-resolution graphics displays. The result will be the same as in the small computer market as a whole, namely, steadily (and sometimes precipitously) declining prices for a given level of perfor-

mance. In 1983, the leading-edge products offered 1024 × 1024 pixels (picture elements) with multiple memory planes for color or levels of gray scale, and/or multiple windows for alphanumeric display. In the near term, most of the effort in graphics terminal design will be focused on information processing capability rather than on increased resolution. The standardization efforts referred to in the previous paragraph, encouraged by the insistence of the US government that a unified graphics database be used on government projects, will result in VLSI controllers for standard functions, while very-high-speed image processing requirements appear well suited to bit-slice microprocessor implementation.

Printers and plotters

Printers can be divided into two broad categories: fully formed character and dot-matrix printers. The ink-jet printer is a special case of the dot-matrix category and, after a long gestation period, is beginning to penetrate the low-end market. At the low end of the product spectrum in each category, the RS-232 and Centronics parallel interfaces are ubiquitous, with the RS-232 interface also being employed across the full spectrum of printer and plotter products. With the appearance of low-cost color capability, the differences between dot-matrix printers and plotters are diminishing.

Fully formed character printers fall into two categories: character (typically, daisywheel) and line printers. Character printers are utilized for high-quality output and are divided into low-cost products operating at 15 to 25 characters per second and higher-priced units in the 35- to 55-character-per-second range. Prices in both categories declined significantly in 1983 and are expected to continue to do so. The garden-variety low-end products differ little from their higher-speed cohorts and may well disappear under the price pressure. The key design trends appear to be the adoption of standard components (ribbons and printwheels, etc.), the addition of enhancements such as microjustification and super- and subscript capability to the low-end products, and increasing emphasis on nonimpact (ink-jet, thermal, and laser) print technology. Nonimpact techniques appear to hold the key to very-low-cost printers in each performance range.

Line printers are moving up from 300-, 600-, and 1000-line-per-minute levels to 400, 800, and 1200 lines per minute, and prototypes of 2000-line-per-minute printers are becoming available. Band printers continue to displace the familiar drum and chain printers in all but the most demanding (in terms of duty cycle) operations. One of the most interesting new printer products is the low-cost laser printer introduced by Canon, Inc., early in 1984. This brings high speed, high quality, and mixed text and graphics output capability within reach of desktop microcomputer systems.

Developments in dot-matrix printers are moving in two directions—increased print quality at the low-speed (40- to 80-character-per-second) end and increased speed at the high end. Standard 7 × 9 and 9 × 9 dot-matrix printers began moving from the 80- to the 160-character-per-second level in 1983, and further increases in performance are to be expected. Most low-end dot-matrix printers include graphics capability, and products are being refined to provide multiple fonts, smoothing (by means of incremental shifts in the paper and/or printhead), and other enhancements. Combined friction and tractor feed is becoming standard. As with the other peripherals utilized in the personal computer market, prices are falling rapidly, and the intensive search for low-cost printheads and transport mechanisms is expected to result in further reductions.

At the high end, 1983 saw the emergence of 600-character-per-second dot-matrix printers, a category that is expected to increase rapidly under the influence of the increasing demand for high-speed print capability in small computer systems. These products are expected to evolve into sophisticated, combined alphanumeric/graphics printers that will compete with ink-jet and plotter products. Considerable research and development efforts are being made by several Japanese suppliers in the area of ink-jet printers and, in particular, in color ink-jet printers using multiple nozzles. These efforts are expected to lead to higher-resolution products providing close-to-photographic quality. Dot density will double from the present 120 to 150 dots per inch, and speed will increase to 20,000 dots per second (about 200 characters per second) on products now approaching production.

Low-end pen plotters, with the same RS-232 or Centronics interfaces found in the printer market and providing from two to six pens and an 8½ × 11-inch field, were being offered at the $1000 level in 1983. Like the low-end graphics terminals referred to above, these products satisfy a demand created by the personal and small business system market. Their advantage over the dot-matrix printer is that they can produce higher-resolution output. Whether this benefit will prove to be sufficient to justify the purchase of a dedicated piece of equipment by the mass market remains to be seen. Aside from the cost issue, there are only so many boxes that can be put on, in, or around a desk. At the high end of the plotter product spectrum, higher resolution and greater plotting speed are expected to remain the key design goals.

Communications and local networks

This review of communications and local network peripheral trends does not consider developments in the interconnection media themselves. Only the peripherals connecting the computer to the network are considered, together with overall trends in communication techniques.

Dial-up communications capability is becoming a standard feature of personal computers and small business computers. Integrated 300-baud modems (Bell-103-compatible) were incorporated into several low-end products introduced in 1983, and the acoustic coupler became a thing of the past. The key trend in the modem field is the switch to Bell-212A-compatible units. These provide 300- and 1200-baud, synchronous and asynchronous communications capability and permit use of communications network architectures such as SNA. As local processing capability goes up, the nature of the typical communica-

tions transaction will become increasingly block- or file-oriented, further encouraging the use of synchronous communications.

The Bell 103 modem capability was available in a single-chip implementation from several suppliers in 1983, and volume is expected to rise dramatically in 1984. By 1985, however, highly integrated implementations of the Bell 212A and its CCITT equivalent (V.22) are expected to be available and to be incorporated into most small computers. Low-cost board-level implementations will provide the same capability for installed systems. New modem designs incorporate features such as dynamic equalization, extensive local and remote loop-back diagnostics, local storage of frequently called numbers, automatic send/receive, and security. At the high end of the performance spectrum, fully integrated FSK modems operating at up to two megabits per second are expected to enter production in 1984.

SNA can be expected to evolve from a terminal-to-mainframe network protocol into a generalized computer-to-computer one.

In the multiplexer field, microprocessor-based statistical multiplexers have entirely replaced the traditional minicomputer-based data concentrator and have made major inroads into the frequency-division and nonstatistical time-division multiplexer markets. As might be anticipated from the foregoing comments on trends in modem design, statistical multiplexer design is moving towards enhanced support of synchronous communications. Clearly, this presents a challenge, since synchronous channels cannot themselves be statistically multiplexed (no pauses between characters), at least not in the conventional sense. Various strategies, ranging from bandwidth splitting (where part of the bandwidth is permanently assigned to synchronous channels) all the way to what amounts to buffering the data portion of the incoming bit stream, are being adopted to deal with this problem. As the use of synchronous communications increases, all-synchronous, protocol-oriented multiplexers can be expected to appear.

Another key trend in multiplexer design is the one away from the traditional stand-alone implementation. Like the modem before it, the multiplexer appears destined to become first a board-level subsystem in multiprocessor computer system implementations and then, ultimately, a coprocessor. An integral, communications-multiplexing coprocessor is attractive as a direct interface between individual line buffers in system memory and a high-speed communications link.

Communications controllers. The performance and capabilities of communications controllers are increasing to encompass standard protocols at ever-higher throughput rates for dedicated communications channels, with one-megabit-per-second capability readily available in 1983 and 100-megabit-per-second protocol controllers in design. Support of the X.25 packet-switching protocol and of the IBM SDLC protocols needed to utilize SNA are included in many of these products and are expected to become standard. These controllers are designed to operate in conjunction with the microprocessors utilized in microcomputer systems, and typically incorporate microcontrollers of their own. The trend is towards providing more of the protocol functions within the controller, thus reducing the amount of specialized software needed at the system level. Progress in this direction depends upon the development of standards for the upper five levels of the ISO Open Systems Interconnection reference model.

Because of the overwhelming presence of IBM 3270-based communications networks, the large number of personal and small computers being purchased for use within large companies, and the expectation that the vast majority of IBM installations will be utilizing SNA by 1986, that protocol is anticipated to be the most widely used one. Such wide use will be facilitated by the availability of the low-cost, synchronous modems referred to in the previous section, and implies a significant decline in the use of asynchronous communications. SNA itself is expected to evolve from a terminal-to-mainframe network protocol into a generalized computer-to-computer one.

Like the multiplexers referred to in the previous section and the network controllers discussed below, stand-alone communications controllers (such as cluster controllers and data encryption devices) are destined to become first board-level subsystems within distributed-control multiprocessor systems and then, ultimately, coprocessors.

Local networks. The spread of distributed processing and the large amount of current communications activities that are carried out in local environments (80 percent, according to some estimates) have engendered tremendous activity in local-area networks. These are differentiated from wide-area networks such as the public switched network and the specialized carriers. Usage has been growing and a number of largely incompatible network products are being offered. Although it is not clear that a local network needs, necessarily, to be compatible with any other, the level of support available for widely used networks is an important consideration. De facto standards are expected to emerge during 1984, and the market will consolidate around them. Local networks frequently need to be linked to wide-area networks, and this will typically be achieved through use of the X.25 packet-switching protocol standard.

There are three primary methods employed to implement local networks—baseband, broadband, and PABX-based. They differ in the medium employed to transmit information—coaxial cable for the first two and standard telephone wiring for the PABX-based methods—and in the control mechanisms employed. Dedicated-medium, ring- or bus-type networks employ distributed control at

each node, whereas the star-type PABX networks rely upon centralized control.

Broadband networks have much greater capacity than the single, typically 10-megabit-per-second channel provided by baseband, and offer the potential of carrying voice, data, and video information on a single coaxial cable. Unfortunately, the need for frequency-agile modems is a disadvantage and, unless they become relatively inexpensive, the baseband approach is likely to be more widely used.

With the well-established trend towards combining voice and data handling in PABX design (and the acquisition by IBM of independent PABX market leader Rolm Corporation), star networks seem certain to coexist with CSMA/CD (carrier-sensing multiple access with collision detection) and token-passing dedicated-medium implementations. PABX-based networks have a major advantage in that the physical link is already installed in most cases and relatively easy to install when not, but they lack the performance of dedicated-medium networks. The need to wire the local environment with coaxial cable—50-ohm for the leading CSMA/CD proposal and standard 75-ohm TV cable for token passing—is a drawback.

Because token passing is a deterministic method of providing access that guarantees service while CSMA/CD is probabilistic and falls down under heavy loads, the former will be preferred in situations where response time is important. Although this generally will not be the case in the general-purpose market, where networks are being heavily promoted, the clear indication that IBM intends to support token passing rather than CSMA/CD implies that both will be actively marketed across the board. VLSI controllers for both have been developed, with the Ethernet CSMA/CD approach being the beneficiary of most of the design activity to date.

Ethernet was, in 1983, the closest thing to a de facto standard, and forms the basis of one of the IEEE 802 network standard proposals (the other being a token-passing implementation). The IEEE proposal contains some fairly significant differences from the original (1980) Ethernet proposal and seems likely to form the basis of the long-term standard, which will affect designs frozen prior to the end of 1982. Single-board Ethernet controller products were available from several suppliers in 1983, and the first, typically two-chip integrated controller circuits had begun to appear. Once the confusion over just what "Ethernet" and IEEE 802.3 really are settles down, the level of support should rise rapidly. Broadband support and utilization are expected to lag baseband and will probably not take off until IBM introduces its product(s). The next major trend in networks will be the development of fiber-optic cable-based systems. These, the first of which began to be discussed in 1983, offer the promise of very high bandwidth and throughput.

Other peripherals

Voice input/output technology has received a good deal of attention in recent years, but has not really had an impact on computer systems. Speech synthesis (voice output) has been successfully employed in industrial, consumer, and telecommunications applications, but has had little direct application to computer systems. Voice recognition, which could, for example, provide a simple command-and-prompt mechanism replacing mouse or touch-screen interaction with displays, has suffered from the sheer difficulty of the data acquisition and pattern recognition problems involved. However, the two chief difficulties, speaker-independent and continuous-speech recognition, do not apply to this application.

Low-cost voice recognition chip sets are available from a limited number of suppliers, and others are expected to follow. Several manufacturers now offer plug-in voice I/O modules based on widely used backplane buses, and integrated product offerings from microcomputer system suppliers can be anticipated in 1985. One of the things, aside from cost, that has inhibited the acceptance of speech recognition is the failure to integrate the capability into a useful application, and it is for this reason that stand-alone or add-on implementations are not expected to be widely used.

A potential application of voice recognition that does not rely upon speaker independence, and in fact requires speaker dependence, is speaker verification. This is expected to find use in a variety of security applications, particularly in identifying the users of dial-up computer facilities. In this scenario, a prospective user dials in, calls up his or her voice pattern (through either a sequence of tones or a limited speaker-independent vocabulary), and is positively identified. By using speech synthesis to lead the caller through the identification process, the system makes it unnecessary for the caller to know how to proceed or to even know that voice-pattern identification is being performed.

The major application for voice input/output, however, is in voice store-and-forward messaging, which will benefit greatly from the application of speaker-independent, continuous-speech recognition. Speaker verification also applies here, as a convenient way of identifying the caller and, possibly, the recipient. Some speaker-dependent, continuous-speech store-and-forward systems are being marketed, but their cost and performance are inhibiting widespread use. Research and development efforts are continuing at a number of companies, and the capability of voice input/output peripherals is expected to increase steadily. These improvements in performance, and the accompanying cost reductions, are expected to result in voice I/O becoming a common feature of small computer systems during the second half of the present decade.

The other major "other peripheral" category is measurement and control. Developments in this area tend to get overlooked in the flood of computer-oriented technological progress, but they remain important nonetheless. One of the key application areas for microcomputers is the so-called reindustrialization of the developed nations, particularly the US—hence, analog-to-digital and digital-to-analog coversion will remain vital in the laboratory and in industrial automation. Advances in linear circuit technology have been combined with the ubiquitous microprocessor to put high-performance analog I/O subsystems, capable of providing sophis-

ticated measurement and control functions, onto single boards.

A broad range of these board-level subsystems is available for each of the de facto standard small-computer bus structures. As the techniques for combining analog and digital circuitry on a single chip develop, these subsystems too will become coprocessor components. In a departure from digital circuit implementations, however, the reduced size and cost of these subsystems will be utilized to place them as close as possible to the source of the typically low-level analog data rather than to integrate them into computer systems. Communication between subsystem and host will usually occur via a serial link.

The mass storage and input/output needs of microcomputer systems are driving the development of a broad range of peripheral products. Fortunately, the capabilities of all the products appear to be advancing at quite compatible rates, and there is little reason to doubt that this will continue for the foreseeable future. ■

Andrew Allison is a native of the United Kingdom and has lived in California since 1968. Educated as an electrical engineer, he has been an independent consultant to management on small computer technology and markets and a Dataquest associate since 1977. He specializes in the evaluation and development of mini- and microcomputer-related products, markets, and technology, with particular emphasis on strategic planning. Before starting his consulting practice, Allison spent over 10 years with Digital Equipment and Rolm Corporations, and two as MOS microprocessor marketing manager at Advanced Micro Devices.

During four years (1977-1981) of active membership in the IEEE Computer Society's Microprocessor Standards Committee, Allison made significant contributions to many of the standards developed, including organizing and chairing for its first two and a half years the advanced backplane bus subcommittee. He was also a founding associate editor of *IEEE Micro* and is a senior member of the IEEE and both a fellow and West Coast Branch vice-chairman of the IEE.

After becoming a naturalized US citizen in 1980, he became actively involved in local government and was elected to the Los Altos Hills city council in April 1982, becoming mayor of that city two years later.

Questions about this article can be directed to Allison at 27360 Natoma Road, Los Altos Hills, CA 94022.

The reports of the death of paper have been greatly exaggerated. Not only will computers not halt the flow of paper, they will probably increase it.

The Non-Death of Paper

Roy J. Lahr
Creative Associates

Written information, by its physical nature, can be repeatedly examined. But, because written communication necessarily lacks the face-to-face link present in verbal communication, the writer must provide the background information and sense of immediacy that in spoken communication are provided by nonverbal cues. And because written communication can be repeatedly examined, we tend to be far more critical about the *form* of that communication. In contrast, speech is usually very informal, with the structure provided by the surroundings and by information shared between speaker and listener. Since these two factors may be missing in written communication, it must generally be much more formal, and any deviation from the rules of good writing can interfere with the efficiency of communication. Certainly, a lack of structure that is interpreted as "dead wrong" or "ignorant" by the reader will cause him to rescan the information, and he may assume that the information itself is as defective as its structure. Thus, if a writer sincerely wishes to influence a reader, he must be very aware of structure and style, and even of nuances of form, such as what paper to use and how best to enscribe the information.

From a modern perspective, "written information" means all information already visible to the eye, such as handwritten or typed material, and is coming to include information that is *potentially* visible, such as information stored in a computer or in magnetic memories, since the most common method of first retrieval of such information is by *viewing* it on a CRT display. Written information is also coming to include information derived from computer databases via "category-item" selections. Besides archival storage, a great advantage of electronically stored information is the ease of *re*manipulation it provides the writer, who can vary content or form before creating a final printed page.

The flexibility of using stored information with electronic displays has caused some authors to predict "the death of paper" as an information medium. Such views are sufficiently common that many people easily accept the idea of a "paperless" future. For instance, in his best-selling book, *The Micro Millenium,* Christopher Evans devoted an entire chapter to the subject of the electronic display's displacement of paper-based information.[1] My contrary hypothesis is that far from causing "the death of paper," the ease of electronic manipulation of infor-

0272-1732/84/1000-0018$01.00

mation will instead cause an *increase* in the amount of paper printed each year, although people will give a lesser value to each sheet of paper.

History of writing and printing

Today, with our easier methods of document creation (and copying), we find it difficult to fully conceive the extreme amount of labor that earlier methods of writing entailed.

The recording of information began with tracings or carvings on surfaces. Early man probably made drawings in the sand along rivers or lakes, but the only ones still available to us are the cave drawings showing animals, both live and killed. Even after man could produce metal tools, making written records by carving stone, even sandstone, was tedious. Only simple ideas could be expressed, and the artisan had to have a fixed image of what was to be carved over the long period of production. Drawing with a sharp stylus or a brush with colored fluid on birchbark or an animal hide was much faster, and some early craftsmen made layout drawings on such materials before beginning to carve wood or stone (or sometimes found that the simpler drawings on hide would serve almost as well as the carved versions).

Writing in wet clay (dried or baked for permanence) or on matted fibers (i.e., paper) required a lot less work for the author or his scribe. But, while this made written communication between a few people easier, it did not lessen the difficulty of communicating with larger groups. Yet, as world population grew, societies became necessarily more complex, making it even more important that "the rules" be communicated to the populace. One solution was the town crier method of group communication. This was augmented by the use of prominently posted brush-stroked signs, a method of multiperson communication still used in much of China. The larger letters of such signs could be reproduced easily from carved master "plates," when the same poster was needed for posting over a large area.

However, to make teaching possible, so that people could become more skillful (i.e., "educated"), required some method of making multiple copies of a "master" document such as pamphlet or book. Before Gutenberg's movable-type printing system was widely used (originating in Mainz, Germany, around 1450 AD), the only method of copying a master document was to have several people write it down until the required number of copies were made.

This copying was done in a *scriptorium,* or writing center, where only sunlight was used (because of the danger of fire from lamps). Its cold, damp atmosphere must have been a most unpleasant environment, especially for such a tedious, repetitive task as copying. Working in silence, first smoothing the animal-hide vellum page with pumice stone, then ruling the writing lines, and then weighting down the pages which were to be copied, the

MACINTOSH DRAWING BY ROY J. LAHR

scribe had to be dedicated indeed. Most scribes worked with a pen in the right hand, a knife in the left. The knife was used to sharpen the pen, of course, and to scrape off mistakes, as well as to steady the vellum page near the point at which the pen was to be used (the animal skins were somewhat flexible and could stretch under pen pressure if not steadied). In medieval times, the most common ink was made from oak galls (an abnormal swelling of the tree's tissue due to insect invasion or disease) and iron powder. The ink could not be dried by blotting, but had to be allowed to dry slowly to a deep black. Ink made from iron and oak galls was still in use in Shakespeare's times, and was mentioned in some of his plays ("Let there be gall enough in thy ink, though thou write with a goose-pen"—Aguecheek in *Twelfth Night*).

Keyboard input creates an endlessly mutable "electronic twin" of the information that originated on the piece of paper or in the author's mind.

Because of the labor required for copying, it made sense to use the durable vellums instead of the early handmade, low-quality paper. Fortunately, the papermaking technology that had originated in China in about 500 BC was modified and improved in Europe so that machine-based papermaking became possible. The greater availability of materials from which people could be taught to read and write spread literacy enough so that "portable scribes" came into demand to record business transactions and even common people's events such as births and deaths. These scribes could carry their pens and knives in a case, and their ink in ink horns (often made from cows' horns), which were tied to their belts. However, while these portable scribes were not rare individuals, they were scarce enough that the bulk of their nonreligious writing had to be reserved for business purposes. Business scribes (or clerks) were often so important that they were stationed at high desks, surrounded by vellum sheets, extra pens, ink pots, knives, paper weights, and rulers, overlooking the surrounding business floor so as to be able to take dictation to record the details of each purchase or sale. This was a popular vocation, for many of these business clerk-scribes enjoyed much better working environments than the Church scribes had, since the businessmen themselves had to work in the same area.

When combined with improved versions of Gutenberg's movable type, machine-produced paper made volume production of books and other written materials possible. More fundamentally, the cost barrier to widespread use (and ownership) of printed matter was broken. This in turn served to encourage more literacy. There were, of course, clerical objections and legal barriers raised to this new technology which threatened the Church's previous monopoly over printed matter—over what was to be printed and over who should be allowed to read it. In pre-Renaissance times in parts of Europe, for instance, it was forbidden for people outside the court or the Church to send or receive letters. However, once it had been shown how to rapidly produce books by printing, there was no way to prevent the previously tiny flow of information from becoming a torrent.

Thus, there is a good "precursor" example of the influence of a technological advance upon the practicality of high-volume production and on user demand for the final product. By noting what happened to the distribution of written materials when papermaking machines and movable-type presses became available, we can explore what might happen as a result of advances in electronic word processing and printout capability.

The next major technological improvement that influenced the western world's distribution of printed matter was the faster printing press. (The Gutenberg-style of descending platen was very slow.) With newer types of printing presses, newer methods of making large volumes of good-quality paper were developed, along with new methods of producing printing plates. Of course, Louis Daguerre's invention of photography in 1839 was soon applied to all phases of printing-plate production.

Recent history

The need to be able to rapidly generate transaction paperwork during World War II served to ingrain the typewriter as a standard professional communication tool in the mind of the office worker. And, since many more people knew how to type, the use of the typewriter for personal communication gained acceptance by the general public. Hence, when the need to transfer information copied from a document, or directly from the mind of the author, into computers arose, the typewriter keyboard became the predominant information input system.

It is interesting to note that keyboard input creates an electronic "fraternal twin" of the information that originated on the piece of paper or in the author's mind. Thus, magnetic or electronic memory mimics the information that was (or will be) placed on paper. But, unlike paper-based information, the "electronic twin" is endlessly mutable through the powerful information-manipulation capability offered by computers, even by very small personal computers.

Examining the paper-output side, we can see that in the last decade it has become less common to print output paper at a central site, and more common to employ slower but more letter-quality-like printers at the point of need to print information in compact form on standard-sized paper. In this arrangement, the large, much faster central printers print out only routine summaries that are then transported to the users.

Since the forte of electronic data processing equipment is the processing of information, it was not very long before experimental systems for handling *text* (rather than numbers) were developed. Text was at first processed using punched paper tape as the storage medium, but this type of processing was very slow and difficult.

Text handling (i.e., the word processing, or WP, function) has benefited from the rapid advances in microelec-

tronics that have made complex text processing feasible on single-user microcomputers. Previously, such capability was available only on multiuser mainframes and minicomputers. In addition, these new "personal word processors" can use the newer forms of typewriters (IBM Selectrics or Xerox-Diablo daisywheels) for convenient, "local" letter-quality output.

Another major technical advance in word processing was the "soft" display of electronic information. A "blind" word processor (one that provided only typed paper output to look at) could help the typist more quickly get correct, good looking final pages, since he could type at maximum speed and correct errors by inspecting preliminary printed-output pages, but made the job tedious—the typist had to keep making printouts just to find all the mistakes (wrong characters or improper formatting) in the text. This difficulty was eliminated by adding a display of one to four lines of text, using light-emitting diodes, light-reflective liquid crystals, or vacuum-fluorescent segment lamps, so that the operator could see a line of text *before* it was printed. Though this limited display of stored information was an improvement over "blind" word processors, exploring what a finished page would look like with this type of display has been compared to reading a newspaper through a mail slot—possible to do, but not much fun.

The real advance came with the use of the cathode-ray tube as a visual display unit. CRTs had been used with mainframe computers in the late 60's to display statistical or graphical information and, occasionally, to provide "soft displays" of information to be printed later.

When microchip computers (so-called "personal computers") became available, CRT displays of 80 columns by 24 or 25 lines became very common for word processing applications. However, examination of the final format of longer documents was slow on such limited-capacity displays, since a single page might have up to 57 lines. (Getting a visual idea of a 57-line page on a 25-line screen can take a lot of vertical scrolling . . . not a fast operation.) This problem was solved by the development of "full-page" displays. Though they require a high-resolution CRT system and very-high-speed electronic display logic, these displays are now offered by several manufacturers.

They provide a very practical way to choose among various formats. The operator can see what the document would look like with various vertical spacings (3, 4, or 6 lines per inch), with various horizontal character spacings (10, 12, or 15 per inch, with or without proportional-width spacing), and with or without right margin justification. This tryout before actual printing, both for readability *and* net appearance, can be very valuable. It allows the operator to create good-looking pages of almost typeset quality.

Naturally, since a full-page display can show an operator what a final page will look like, it can also be used to examine text files coming into an office from electronic storage elsewhere, eliminating the need for a separate paper printout. It is this very capability to quickly show what a stored electronic page "looks like" that causes many people to expect that printed paper will soon be completely replaced by "soft" displays.

As a bulk handler of printed paper, the copier is firmly entrenched in business office life in most of the western world and Japan. In Japan, copiers are more necessary than in the west, due to the very high preponderance of *handwritten* originals (which may account for the progress in the Japanese production of copiers and ball-point pens). By contrast, the copier started out in most western countries as a convenience that has gradually become an office necessity. Not only does the copier efficiently make distribution copies of incoming documents so that they may be examined by all concerned, but it may also be used to produce the more ubiquitous social paperwork which ties together the hierarchical office layers of medium to large companies.

Although it is possible to attain approximately the resolution that paper allows on a display screen, it is *very* difficult and not often achieved.

Because of the aggressive development of microchip-based devices, any business office can consider owning a very powerful ensemble of electronic equipment, and an equally powerful group of electronic-mechanical devices (keyboards, copiers, printers), all of which enhance the generation, reproduction, and general flow of information. And while the office has been the major "test site" for these types of equipment, the availability of the personal computer and its peripheral equipment has given the home user (or even the traveling user) the potential of having many of the same WP features that now exist in office equipment. Thus, it is instructive to examine whether paper-based information can be expected to be replaced by the "soft" display capability these home or portable units offer.

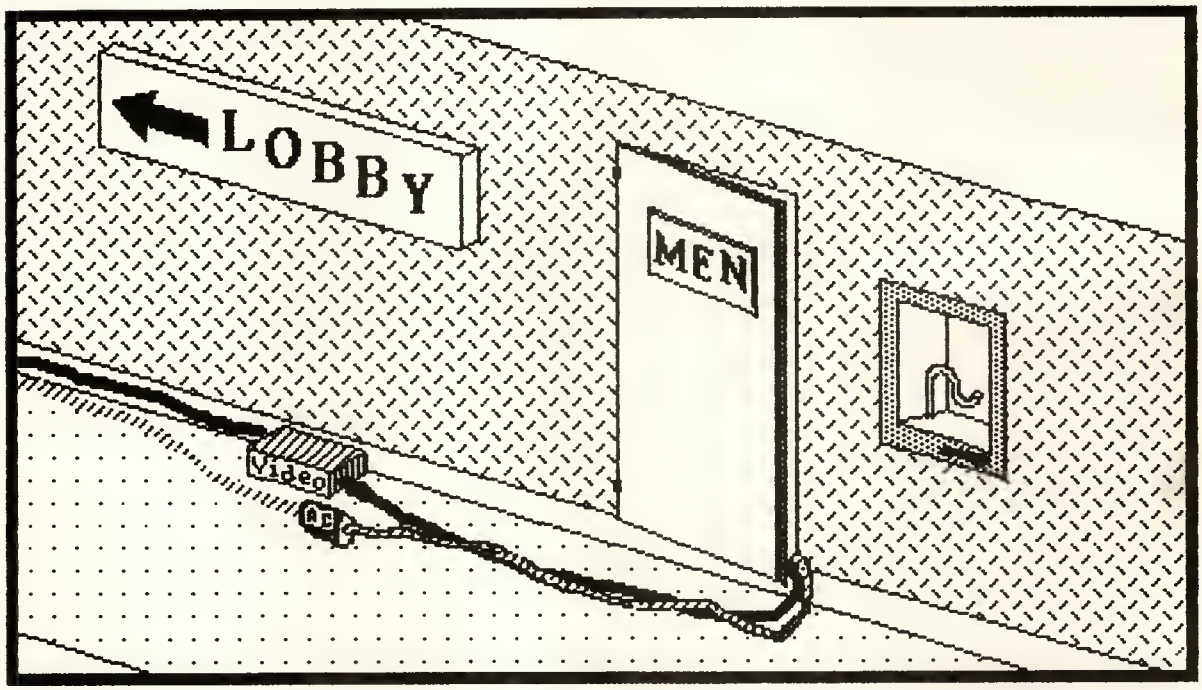
Paper-based information flow: the near-term future

The argument for "the death of paper" is that visual display units such as cathode-ray tubes, liquid crystals, and other potentially high-resolution technologies will displace paper. While it *is* true that all of these display technologies were specifically designed to transform electronic information into a visible form, they suffer from some severe disadvantages when compared to paper. First, although it is possible to attain approximately the resolution that paper allows on a display screen, it is *very* difficult and not often achieved. Let us examine what is possible from a technical standpoint, making a convenient restriction to "black and white" text—i.e., no gray scales, no color. A good offset press (with an excellent master and a top operator) can produce images with a resolution of more than 500 lines per inch. Images in the range of 300 to 450 lines per inch are

usually considered acceptable, although the difference *is* visible, especially if a 300-to-450-line image is placed next to a 500-line one. A video display with 1000 lines vertically is considered a very good display, yet if you are trying to display an 11-inch document with, say, 10 inches of information, you are getting only 100-line-per-inch resolution. If you really push a cathode-ray tube display, using a high-resolution phosphor, dynamic focusing, and a dispenser cathode (for high peak beam current, so you can throw some beam current away in the aperture and focus zone), you may be able to get 2000 lines. This will provide 200-line-per-inch resolution for your document. But to get this, you probably will have to push the CRT drive circuits to somewhere near 100-MHz speed. Only very fast logic circuits can deliver such speed, and there are difficulties in putting such circuits in densely packed arrays, i.e., in VLSI/VHSIC superchips. For the military, where the cost-performance trade-off is not as critical as it is for the commercial world, 2000-line special-purpose displays *are* built (together with associated equipment) by Raytheon, Hughes, and Thompson-CSF. Most of these units are used in military reconnaissance applications, where very high resolution is often needed for interpretation of details.

Thus, paper retains a clear advantage over known "soft" display technologies as far as resolution is concerned. So, when people predict "the death of paper," they probably assume that technical progress will rapidly deliver much higher resolution displays having most of the essential viewing characteristics of paper. Unfortunately, designers have been improving CRTs for 25 years, with most of the last 10 years spent wringing out the last bit of performance or cost reduction. Hence, I think it unlikely that the resolution of reasonably-priced displays will rival that of printed paper in the next 10 to 15 years.

The second disadvantage of electronic displays is that they are not usually very portable. While you can take paper anywhere, you would hardly take a large CRT down the hall to show someone something. It is true that if an office had a local-area network, and two workers each had his own terminal, one could show the other a page of information by sending that page to the other's terminal. Such local-area networks, and the provision of terminals to all professionals in an organization, are hardly common yet, and my estimate is that in 10 years about 15 percent of all office professionals in offices with more than 25 people will have a networked terminal, and in 15 years, 20 percent. These estimates are based on the cost of installation and the types of jobs in which there is a satisfactory payoff to financially justify the installation. So even if we restrict the examination to office pro-



MACINTOSH DRAWING BY ROY J. LAHR

What are they? Those are just the extension cables for Bill's display monitor. He just can't stand to go anywhere and relax without taking something along to read.

fessionals 15 years out, my estimate is that less than 20 percent could realistically contemplate a largely paperless office. When one examines the need to be able to look at documents without having to convert them into electronic form (incoming mail), and the costs of converting documents and filing them on, say, a large optical disk, it is clear that one will still need to be selective about what is brought into electronically-processable form and what stays on paper. What of information outside of the office? You can only bring a terminal with a very limited page-display capability on the bus or train and read information on the way home. And, since the cost of large displays is geometrically higher, it is not likely that compact, full-page displays will be affordable before the late '80's.

I certainly agree that information mutability is the very reason to use a visual display unit such as a CRT, liquid crystal, or LED display—for *composition* of information. But I would postulate that most information created on a VDU is targeted for printing on paper, if the reader's potential interest in receiving or acting on that information is more than very temporary. Further, nearly unlimited mutability makes it very likely that many revised versions of documents will be created. People will want to add to documents, suggesting changes, giving amplifying examples, or providing references and, in many cases, will want their versions to be available to others. If the capability to easily make changes is widely accepted, there will be much more frequent invitation to add comments or suggest changes. With such changes or additional comments in place, the modified document will become, in effect, a multiauthor document, essentially replacing the single-author original. Mutability, then, *encourages* document creation by nearly simultaneous participation (all on-line, with network interconnection, or all receiving printed output and thereupon revising it). Multiauthorship of documents, though now cumbersome, will be encouraged both by social pressures and technological improvements—multiauthor, revised documents may be considered "richer" (from an information-content standpoint) than the plain originals, for example. Obviously then, this flexibility and ease in making annotations will cause the generation of more versions of documents, with the further likelihood that a larger number of paper copies will be printed out for examination off-line.

One very valuable attribute of VDUs is that beyond their obvious advantages in document origination, they provide an excellent "browsing" environment in which one can read short messages and briefly scan longer, multipage documents (or read summaries of them, if available), and then target some of these materials for printout on paper, to be read later. Again, the existence of VDUs, rather than causing "the death of paper," will instead cause *more* paper to be printed, since it will make browsing in very large stores of information so much easier. For instance, with some keywords or key phrases, a VDU user can sort and collate information from a large store of material, and is much more likely to want to see such information when he knows that it fits his criteria of "what's important." Many professionals get so many magazines that it is hopeless to contemplate reading *all* of each one that arrives. Thus, there is often the frustrating realization that one may easily miss something important. If such magazines came either with an "electronic twin" or, at least, with an index in electronic form, a sort of *all* the articles in *all* the magazines could be made on the basis of keywords or key phrases that represented the user's interests. He could then browse through a list of potentially useful articles, seeing whether, in fact, there *was* much of interest. If there was, paper copies of the selected articles could be printed out. And, although manual keyword tagging of the content of articles or books is a tremendous labor, there are encouraging signs that artificial-intelligence-based computer scanning for keywords may be possible toward the end of this decade. Progress in AI is slow, since discovering just what constitutes "meaning" is often in exact, and also frustrating, since it is extremely difficult to duplicate the human capability to relate new items of information across an enormous range of old information. While a computer cannot "forget" a fact (assuming memory and circuit integrity), as humans can, machine methods for cross-comparing facts so that they can be categorized and assigned an information value are still rudimentary. Rudimentary or not, the possibility of saving a great deal of labor and of creating better ways of filtering information from the bewildering amount we are all presented with is so attractive that research in AI methods will continue to receive heavy support. The moment we readers are presented with better ways of filtering information, the more likely we will be to make use of that facility (so we don't miss anything), and the more likely we will be to demand paper-based printouts of the selected information so that we can read it. Thus, the probable result is *more*, not less, printed paper.

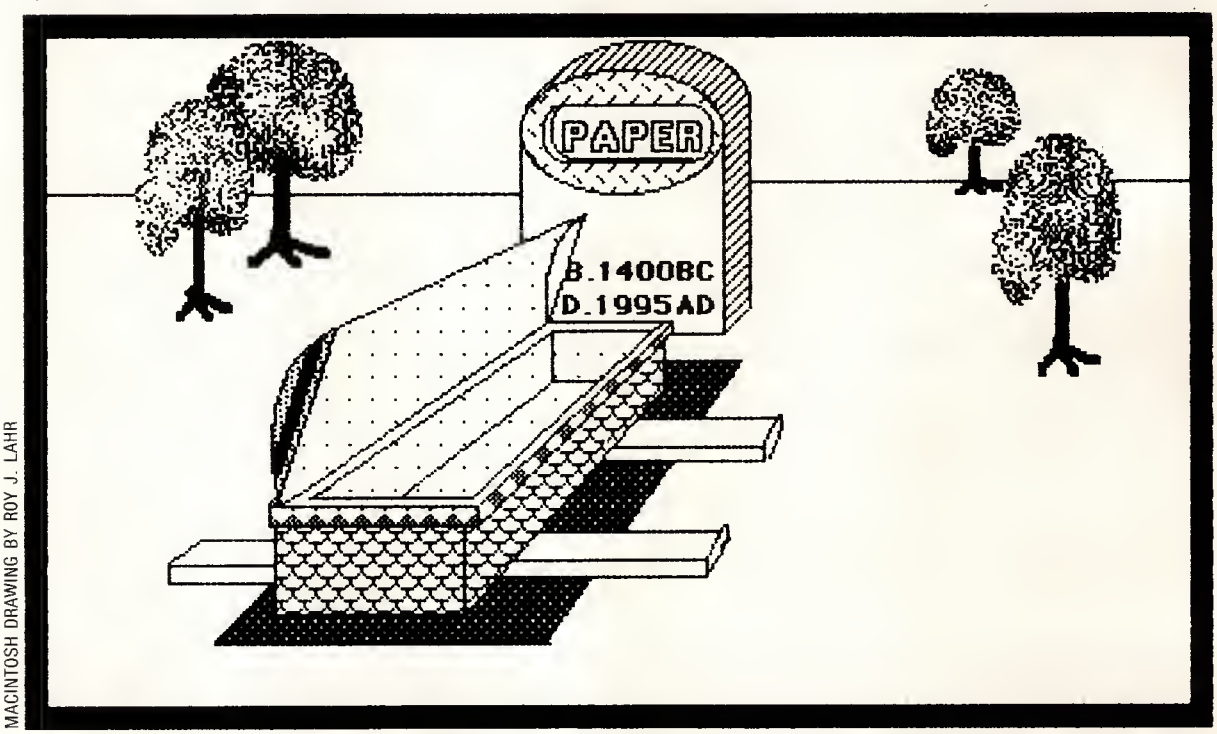
It can be asserted that AI-based information processing is potential rather than actual. Nevertheless, there *are* some very advanced information handling systems in active use that we can examine. One is the interconnected network-terminal-file-printer system in use at the Xerox Research Center in Palo Alto, California. There, most of the several hundred professionals and secretaries are provided with an "Alto" terminal having a very fast processor, an 890-line screen, local storage, and a network connection port. The network is Xerox's Ethernet, which is offered by the company commercially with its Star (Model 8000 series) terminals. The Ethernet is a fast network—it allows message transfer between points at a 10-megabit-per-second rate. Backing up the network are central facilities that include a very large computer (custom-built, but similar to two Digital Equipment PDP-10s, back to back) and substantial disk storage; also supporting the network are laser-xerographic printers located throughout the building and interconnection gateways to some 1000 other Alto users throughout Xerox and in a few test-site universities. This ensemble is a good model of the sort of hardware that other companies may soon be able to buy, either from Xerox or from other vendors. Naturally, the Xerox Research Center has a standard mailroom and many standard Xerox copiers located throughout the research complex. The 1979 print volume from the laser-xerographic bulk printers, printing *only* information desired by the Alto terminal users, was

estimated at over 1,000,000 sheets, *without* any reduction of the previous copier work load and with a steadily increasing mailroom volume. This volume does *not* include the printout from local or experimental printers, and so this *additional* amount of paper printed is persuasive evidence that "the death of paper" will not occur and that, in fact, *more* paper will be the likely result of electronic information handling.

An "author's terminal," which would involve a somewhat altered combination of these new technologies (visual display, text processing, and complete hard-copy printout facilities), has yet to appear in other than wholly experimental form. "Direct-to-VDU" composition, with paper coming into existence only *after* the page image on the VDU is considered satisfactory, is different in function from that performed on the more common WP terminal, on which the operator is usually recording input from a voice tape or pre-existing paper document. An "author's terminal" would give the user nearly unlimited ability to manipulate information, and the form and content of the output document would be limited only by his originality and patience. In addition, he could readily transmit this document to others, either for comment or as a "currently final" version.

New input systems, in particular voice-assisted terminals in which the keyboard will play a more limited role, will become available. And perhaps academic or industrial research will discover new and more powerful voice recognition algorithms which will make large-vocabulary, speaker-independent voice recognition devices more achievable. Otherwise, equipment developers will have to depend strictly on "pounding the problem to death" with substantially more electronic (superchip) capability and on constructing large lexicons, with AI-based context-guessing capability. However, the widespread desire for such equipment, and the difficulty of convincing business executives that they should learn to type, will continue to motivate researchers in the field.

But until the mid-1990's, when such voice recognition equipment is likely to be available, anyone who does not type is hampered in trying to transfer his thoughts into his local information handling terminal. Fortunately, the popularity of computer classes in schools has increased the desire to learn to type, so keyboard training classes now attract students from beyond the customary groups—the secretarial students who wish to learn to type office documents and the college preparatory students who know that a typed paper often gets a better grade than even the most nicely handwritten one. Thus, a much larger body of "keyboard-capable" people is growing up than exists in business and industry today. The popularity of personal computers with standard keyboards for text



MACINTOSH DRAWING BY ROY J. LAHR

There's no body??? Well--next time I won't make the arrangements until AFTER I see the actual death certificate!

input is, of course, a very potent motivating factor.

Thus, if more people know how to type and how to use computer-based information handling equipment, more people will interact with electronically stored materials and will want printed output. And when voice recognition becomes practical, those who do not now type will be brought into this group of hard-copy requestors, further increasing the demand for paper printout.

It should be noted that the foregoing observations all point to a probable increase in the volume of information put into printed form. History suggests that a newer medium (electronic storage of information, in this case) is used in new ways and does not diminish the use of an older medium (here, paper). My examination of information processing technologies and their probable near-term utilization persuades me that, far from causing "the death of paper," these new technologies will cause a substantial *increase* in yearly paper printout volume.

The rapid development of microelectronic technology enables the easy display of information at fair-to-good resolution. Users can easily browse through electronically-stored documents, and those who receive documents on their VDU-equipped terminals can just as easily add commentary or even make major changes in format. They can, in effect, create *new* versions of the documents. These new documents can in turn be viewed (and changed or annotated!) by *other* recipients. These users will *very* frequently request paper printouts of such "new" documents so they can read them later, possibly away from their terminals. These probable patterns of use strongly suggest that there will be many more requests for printout—that a *larger*, not smaller, paper-based information flow will occur. Perhaps the ease with which paper printouts will be able to be obtained will even lead towards a disregard for the paper documents themselves—having gotten them easily once, users will find it equally easy to recreate them again, particularly if their terminals maintain logs of all printouts made. On this point, there is not yet enough data to do more than speculate. ■

Reference

1. Christopher Evans, "The Death of the Printed Word," Chapter 8 in *The Micro Millenium,* The Telecom Library, New York, 1980 (published in Great Britain as *The Mighty Micro,* Gollancz Pub. Co., London, 1979).

Questions about this article can be directed to Roy J. Lahr at Creative Associates, PO Box 69445, Los Angeles, CA 90069.

This device consists of intelligent building blocks which may be assembled by hand and then automatically queried by computer. In this way, a structural database can be quickly and easily created.

A New Peripheral for Three-Dimensional Computer Input

P. D. Noakes
University of Essex

R. Aish
Ove Arup and Partners

The problem of entering three-dimensional information into a computer has been of considerable interest for many years. Early attempts involved the separate digitizing of two or more two-dimensional views of the object. For example, in 1974 Sutherland reported the use of a multipen digitizing tablet which allowed simultaneous digitizing of two-dimensional views to produce data which were then transformed to produce orthographic or perspective views.[1] Allison and Greenberg reported in 1978 the use of a powerful three-dimensional editor with two-dimensional plans to produce three-dimensional geometric information.[2] In both these systems conventional two-dimensional drawings must be produced for each object if it is to be successfully represented in three-dimensional form using the powerful computer graphics facilities currently available. An alternative method of entering three-dimensional information is to use a 3D sonic digitizer such as that produced by the Science Accessories Corporation.[3]

In some applications, however, the object may be designed by producing an actual physical model. An example of this is often seen in the automobile industry, where the prototype body shape of a new vehicle is produced by forming a full-sized clay model which can be fully wind-tunnel tested to establish the drag figure associated with the design. The final body shape of the model is then used to produce working drawings. Computer-assisted production of these drawings is possible if the three-dimensional model can be directly digitized. One method for entering three-dimensional information from a model uses a transducer which is placed in contact with the model and systematically traces its contours. Alternative noncontacting techniques use echometric, reflectometric, or stereometric techniques involving sound, microwave, or light sources and detectors. Posdamer discusses a prototype laser-based stereometric system developed to investigate this principle.[4]

Models are also a well-accepted method by which architects and engineers represent and evaluate alternative design proposals. Although some models attempt to represent detail with a high degree of accuracy, they are generally static representations of particular alternatives

0272-1732/84/1000-0026$01.00

and have not been considered a dynamic part of the design process until recently. Aish proposed in 1978 a flexible modeling system for architects which would also act as an input device to a computer system.[5,6,7] In this system the user-generated model becomes "machine" as well as "man" readable, allowing the designer to readily generate and edit a three-dimensional representation of his design. The important extension required to the modeling kit which facilitates this is the inclusion of an electronically encoded "label" within each element. The mechanical links between the elements then provide a simple communication system which connects through to the baseboard on which the model is mounted and enables the associated computer system to scan the model and generate a data file describing the topology of the model. This data file can then be used to produce, for example, perspective views of the model, two-dimensional working drawings, and bills of quantities, or be used by engineering software to carry out structural and energy analysis. Figure 1 is a block diagram of this type of system, with which the user can readily set up a properties file which associates particular characteristics with each unique element label.

This article is concerned with the principles of operation of such a three-dimensional input peripheral, and discusses the design and performance of a prototype system which has been designed and built in order to demonstrate these principles.

Principles of operation

In concept the interrogatable elements can be modeled in any physical shape or form. However, in order to facilitiate a discussion of the principles of operation of a such a peripheral, we will assume that the building elements have a square or rectangular cross section with their length and width being an integral multiple of some basic reference unit. In addition, when these elements or blocks are mechanically connected, we assume that an electrical connection is also formed.

The constraint of having a limited range of building elements may seem at first sight to be a significant limiting factor to the use of such a peripheral. In fact, this is not true, since by rescaling the physical significance of an element in its database, a computer can represent a discrete building brick at one moment and a complete room at another. Also, it is the user who indicates to the computer the actual scaling to be used to relate the size of the element to the actual physical size of the object being modeled, and allocates the properties that are to be associated with that element. Thus, the basic elements may first be used to build a wall which may have certain characteristics derived from those allocated to the basic wall element. The collective physical and geometric properties of the elements forming the wall may then be assigned to a single element. The user can then assemble a number of these "wall elements" to build a room.

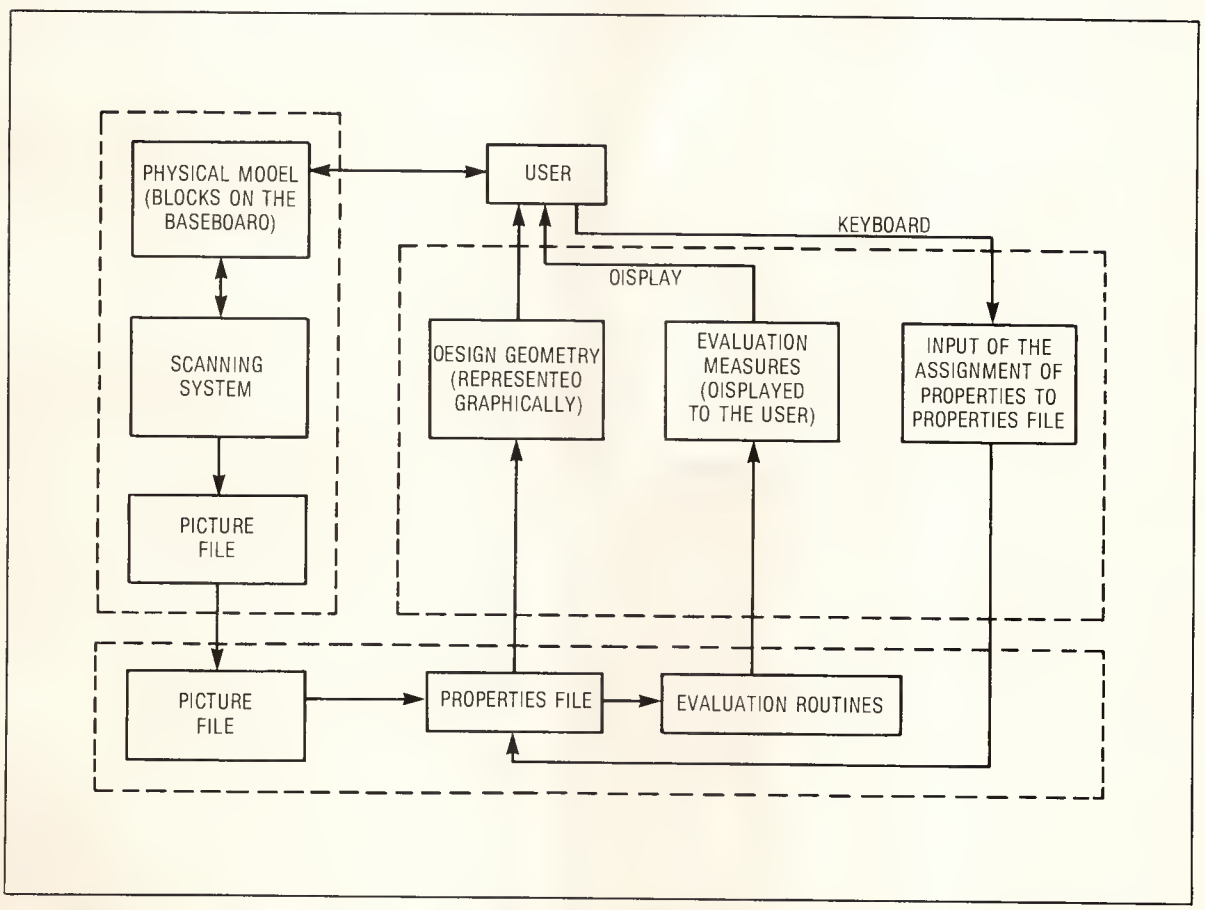


Figure 1. 3D modeling system as an input device to a CAAD system.

Similarly, the collective physical and geometric properties of the elements forming the room may then be assigned to a single element. The user can then assemble these "room elements" to form a complete building. This hierarchical structure allows the physical properties of the building to be defined at any level while allowing the use of the same set of basic interrogatable building elements.

A typical structure using this type of building element is illustrated in Figure 2. This diagram includes examples of a number of structural configurations with which a peripheral of this type must cope. These can be identified as follows:

- Elements can be inserted in a variety of orientations with respect to the baseboard. (In the prototype, the number of orientations is four—i.e., 90-degree spacing is permitted.)
- Elements can overhang the element below.
- Elements can be supported at more than one place and form, for example, a lintel, arch, or floor slab element.

If it is assumed that there is an interconnection point at each *x-y* coordinate position, and that the grid size corresponds to the dimensions of a unit size element, then each element, depending on its size, can be interconnected at one or more positions to the elements below (or the baseboard) and to the elements above.

The interrogation of this structure can be represented by a nodal network (Figure 3). Here each element is replaced by a node while its inputs and outputs are represented by branches into and out of the node. In order to ensure interrogation of all elements, all nodes must be accessed. This can be assured if all branches are sequentially traversed using a tree searching algorithm. The speed of this algorithm can be increased if those branches which have already been interrogated are flagged and not reinterrogated. Thus, in Figure 3, node E, having been interrogated via the path A→B→C→D, is not interrogated via the path G→H→I→D, since it is recognized that node D and all the nodes above have been previously accessed.

When interrogated, each element transmits its electronic "label" through the elements below to the baseboard and thence to the host computer. This electronic label is either a unique code for each element or one of a limited range of codes, each of which is associated with a particular set of attributes identified in the host computer's properties file. It also includes information which allows the element's absolute *x* and *y* coordinates, together with its height above the baseboard, to be calculated. For a square or rectangular element, the cartesian coordinates of its vertices, relative to a set of reference axes positioned with their origin at one corner of the baseboard, are found by performing a series of transformations. These transformations use the relative orientation of the element being interrogated to the interrogating element, the output position on the interrogating element, the interrogation position on the element being interrogated, and the physical dimensions of the element being interrogated. It is an iterative procedure commencing at each baseboard interrogating position and working through each of the nodes interrogatable from

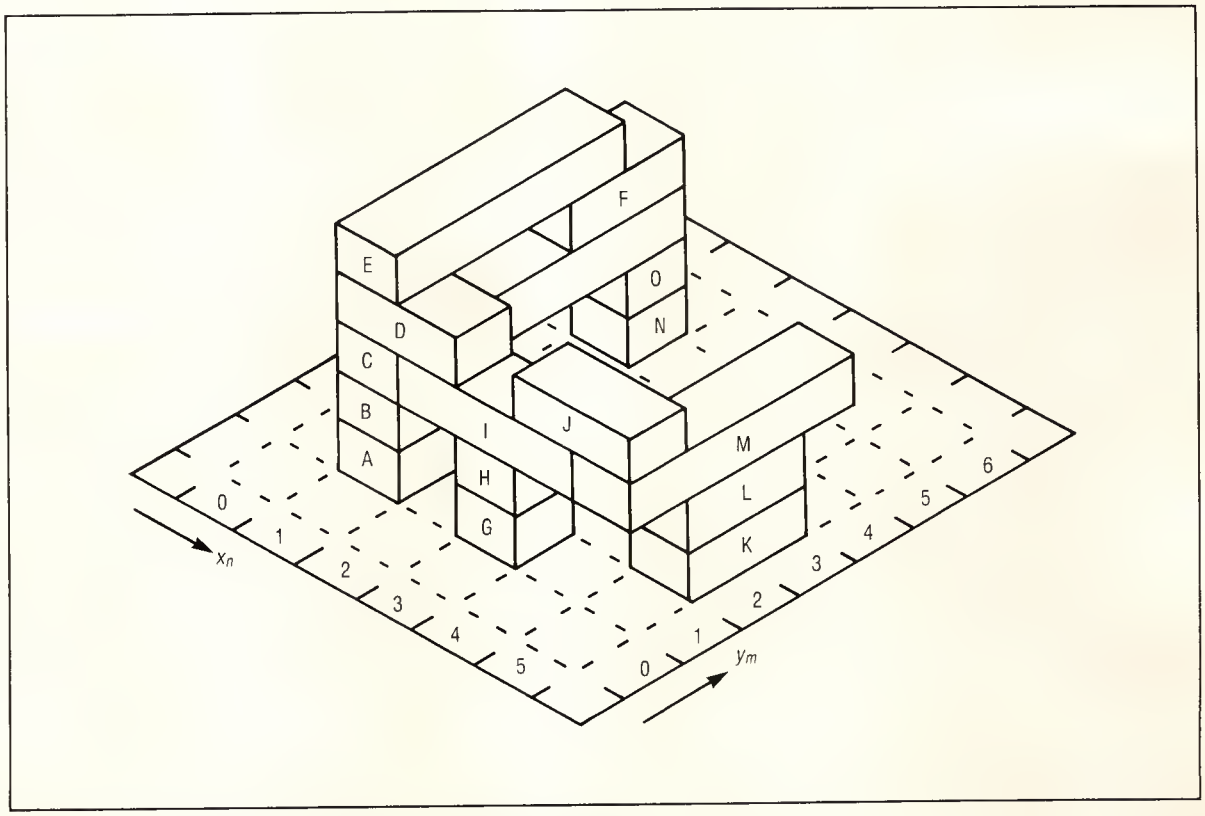


Figure 2. Sample structure built with rectangular elements.

this position. Once all baseboard positions have been interrogated, the data file describing the structure is complete.

System design

The general principles of operation discussed in the previous section give some insight into what is required of the hardware and software. Each element is required to transmit its label when interrogated, as well as to be able to control the interrogation of any elements plugged into it. Therefore it is clear that it must include some processing and control functions. In addition, the baseboard requires some processing power so as to implement the scanning algorithm and to transform the received data into a data file before its transmission over a serial line to the host computer. A microcomputer appropriately programmed for the above tasks is clearly suited for this role.

The method of providing the control and processing capability in each of the elements is not so obvious. One answer is to use a single-chip microcomputer in each element, programmed to respond when interrogated by the baseboard or another element. This solution reduces the problem to a random structure of asynchronously interconnected processors. A solution using this type of structure is under investigation and the results will be reported in due course. An alternative approach utilizes a custom or semicustom VLSI integrated circuit for each element. In this case interelement communication can be synchronized to the baseboard and the electronic labels transmitted synchronously. The current prototype 3D input peripheral uses this type of technique, although the electronics have yet to be integrated in a single chip.

The prototype 3D peripheral

The prototype system is illustrated in Figure 4. Each building element incorporates a synchronous digital system implemented using standard CMOS integrated circuits. The baseboard includes a single-board microcomputer designed and widely used within the Department of Electrical Engineering Science at the University of Essex.[8] This board uses a Motorola 6809 microprocessor operating with a 2-MHz clock (Figure 5). The on-board monitor and the two serial interfaces (both switchable for RS-232 or 20 mA current loop) allow the board to be connected simultaneously to a VDU and a host computer. The entry of a simple code from the VDU causes the board to become transparent so that the VDU can communicate directly to the host computer. The board is designed to be plugged into the department's G60 bus system or to be run stand-alone as in this application. Also included within the baseboard are the microcomputer power supply, a simple interface board, and a separate controllable power supply used to supply the interrogatable elements only when interrogation is being performed (Figure 6).

Before discussing in more detail the functions of the microcomputer in the baseboard, we should discuss the function and structure of the special-purpose electronics designed and implemented in CMOS for inclusion in each building element.

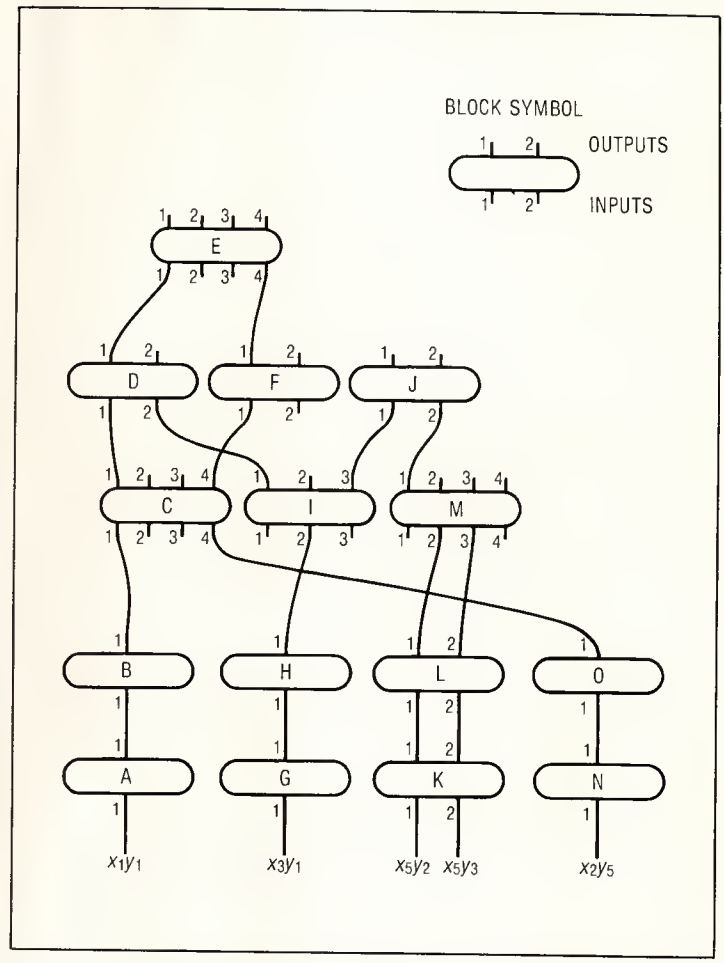


Figure 3. Nodal network representation of the structure in Figure 2.

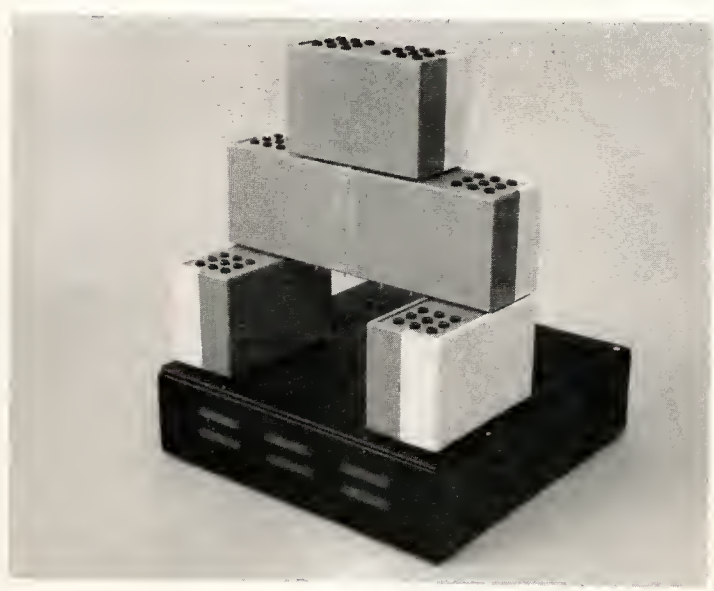


Figure 4. Prototype 3D input peripheral.

Design of element electronics. From the general operating principles discussed above, we can see that the electronics is required to generate a code which includes the following information:

- the element size (height, width, and length relative to a unit of x or y),
- the input location at which the element is being interrogated,
- the orientation of the element with respect to the element below,
- whether the element has been previously accessed in the baseboard scan cycle, and
- a unique preset label for use by the host computer.

In our prototype system a 16-bit word has been used for convenience. This allows building elements with eight

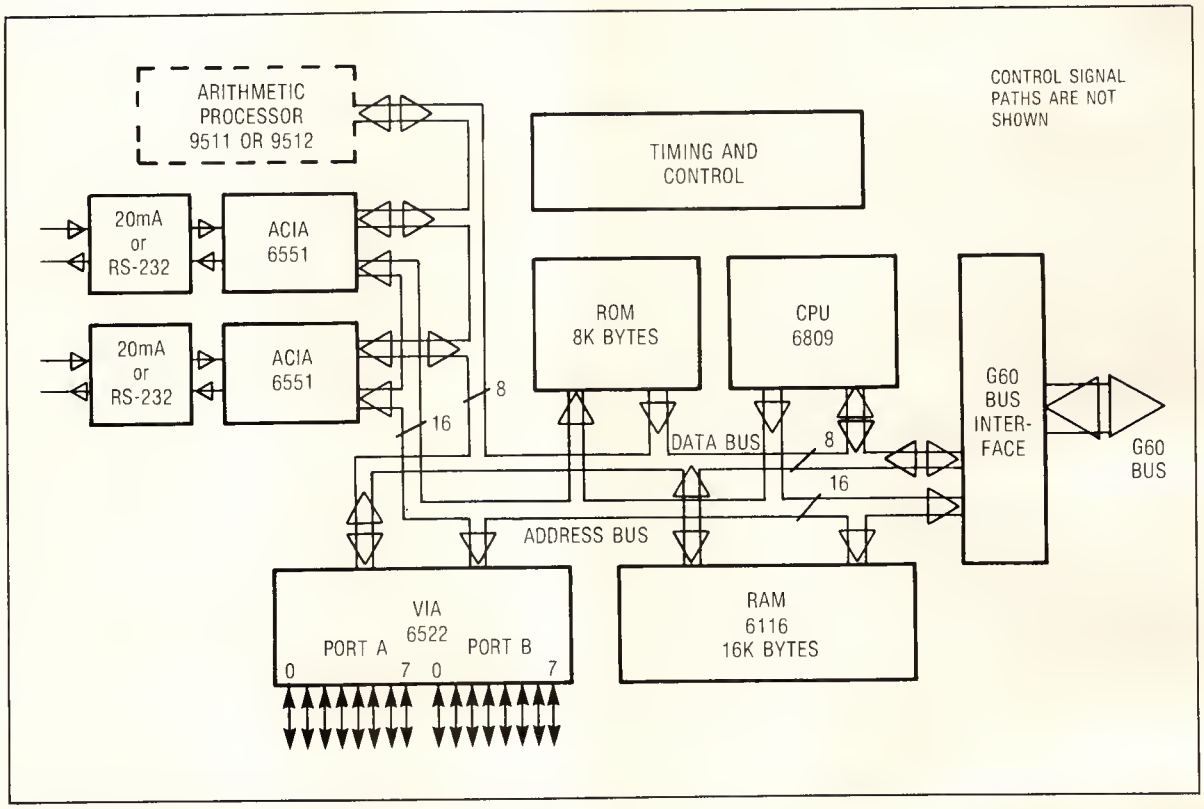


Figure 5. Block diagram of the baseboard microcomputer.

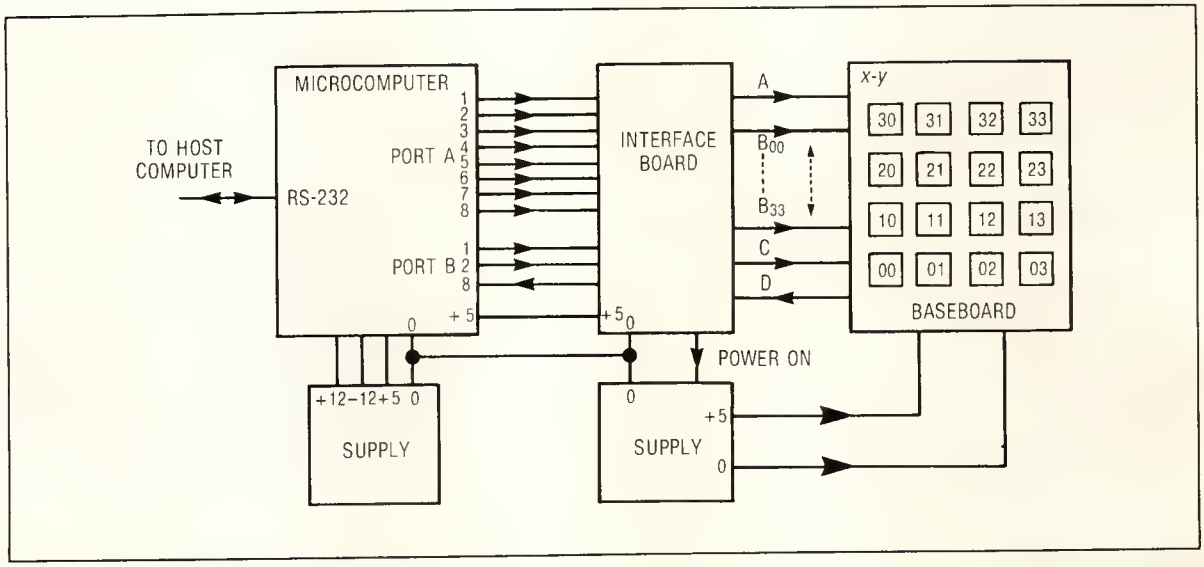


Figure 6. Block diagram of the baseboard.

different lengths, two widths, four heights, and 16 different presettable labels to be identified. Of the remaining six bits, two are used to indicate the element's relative orientation, one to indicate that the element has been previously interrogated, and three to identify the input location at which the element has been interrogated. The number of bits can be readily increased to allow the use of a wider range of elements with different physical dimensions and attributes.

The number of contacts per location can be reduced to three if an internal clock and battery are included in each element. These contacts are used for selecting a particular element for interrogation, for carrying the serial code transmitted in response, and for providing a signal reference. An increase to four contacts per location (plus two for power and earth return if a battery is not used) also provides a convenient method for extracting information about the relative orientation of the interrogated element with respect to the interrogating element. The four signal paths available are used, then, to provide an overall enable (A), a specific location enable (B), an interrogating clock (C, synchronized to the scanning of the baseboard), and a path for serial transmission of the data codes to the baseboard (D). The four contacts at each interrogation point in the prototype peripheral are arranged in a square symmetrically about the center point. The spatial allocation between the reference orientation of the baseboard or building element and the signal paths to the four contacts is identical for each baseboard location and for each output location on the top surface of every element. Rotating the element enables each of the four signal contacts at each interrogation position on the lower surface of the element to be inserted in each of the four contacts on the top surface of the interrogating element or the baseboard. The electronics connected to each contact on the lower surface must therefore be identical. The sequence of application of the three interrogating signals must then be predefined (for example, A-B-C) so that the sequence can be used by the input stage to determine the element's relative orientation to the element below. This determines which of the four contacts on the lower surface should be used to transmit the code to the element below.

Figure 7 is a functional block diagram of the electronics used in the prototype. To implement the requirement discussed in the previous section, input/output processor A uses a sequential logic circuit which derives the orientation and position codes from the interrogation signals applied by the element below (or by the baseboard for the lowest element). The rest of the system is controlled by the system controller and is fully synchronized to the interrogation clock. When the element itself is being interrogated, the shift register is parallel-loaded with an appropriate code that is then synchronously shifted out by the interrogate clock. A flag is then set to indicate that the element has been interrogated, and the element then assumes an interrogating (i.e., a read) mode. When elements above are being interrogated via input/output processor B, the element effectively becomes transparent to codes being transmitted through it to the baseboard; however, each code is also read serially into the element's shift register and processed as discussed below. During this phase, the element is itself implementing part of the tree searching algorithm, since it must establish whether all the elements connected above each element output have been fully interrogated.

The element performs this function by reading in the code currently being transmitted to the baseboard and checking whether the particular bit position allocated to the interrogate flag has been set to a "1". A "1" indicates that either the element has been previously interrogated via another path or there is no element present at this position (all "1's" have been transmitted). If either of these situations is detected, the clock may have to be redirected. However, the elements in the structure above may be of various dimensions, leading to a variety of branches to be interrogated. Therefore, before redirecting the interrogating signals, the element must check whether all the possible branches above have been interrogated. This check is performed by the block-length counter, which adds the length part of the code that has been read in to the currently stored value. This counter is decremented when the interrogate flag bit is a "1". Only when the contents of this counter reach zero have all the elements above this particular output been accessed. The interrogate clock can then be switched to the next output as specified by the contents of the output position counter. If all the output positions have been accessed *and* the block-length counter is zero, then all the elements above have been fully interrogated and the interrogation signals can be removed from the particular element's input.

Each element in the peripheral must of course operate in a way similar to that of the other elements to ensure

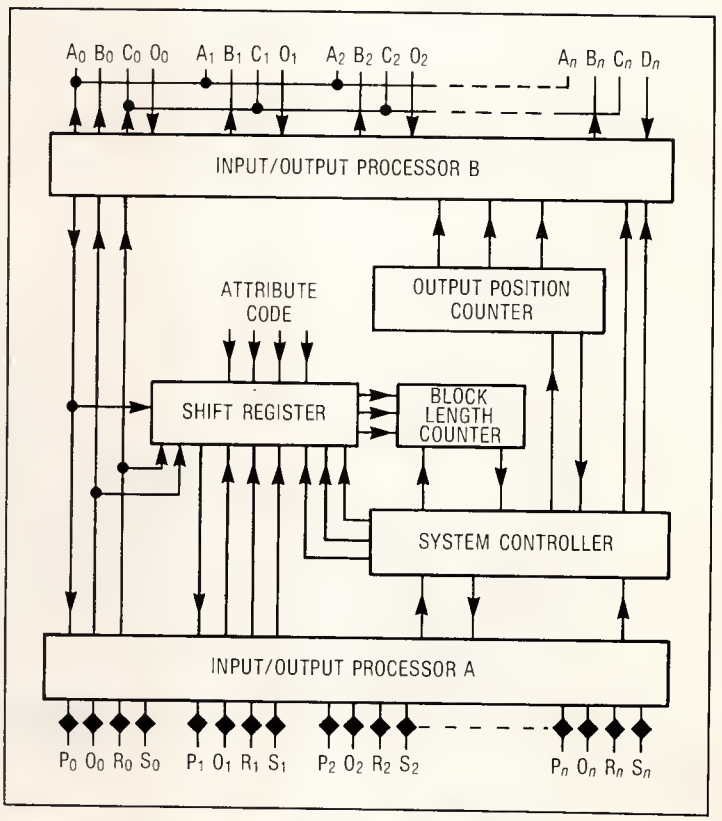


Figure 7. Functional diagram of element electronics.

that every element can be interrogated. A number of prototype rectangular blocks have been constructed with standard CMOS logic elements (Figure 8), and the implementation of the design as a single integrated circuit is now being investigated.

Baseboard software. Having discussed the block electronics, we can now describe in more detail the functions of the baseboard microprocessor. First, it generates the baseboard control signals—baseboard enable (A), *x-y* location select (B), and the system clock (C)—and reads, at the appropriate time, the serial data transmitted from the element currently being interrogated. The frequency and mark-space ratio of the system clock are determined completely by the software, which effectively provides two-phase operation and allows the transmitted serial code to be read midway through each bit period. Second, the baseboard microprocessor implements the tree searching algorithm already discussed. It does this by processing the sequence of received codes in a way similar to that of the element hardware. It is then able to decide when the tree above a particular baseboard location has been fully interrogated and that it can move on to the next *x-y* location. Finally, having completed the baseboard scan, the microcomputer transforms the binary data into ASCII and transmits it to the host computer. The software to implement these functions is stored in an EPROM on the microcomputer board.

Coordinate extraction algorithm. The origin of the absolute coordinate system is initially positioned at one corner of the baseboard, with the x and y axes parallel to its edges. When interrogated, each element provides details of its position relative to the interrogating element. Therefore, in order to establish the element's absolute position in three-dimensional space, an appropriate transform on this data must be performed.

Each element is defined to have a reference orientation (coded 0) in which its x, y, and z axes are coplanar with the reference axes. In the prototype system, each element can be inserted in four orientations with respect to the interrogating element. The three other orientations are coded as 1, 2, and 3 for 90-, 180-, and 270-degree anticlockwise rotations relative to the reference orientation.

The element width and length are each scaled in the prototype to be an integer multiple of the baseboard *x-y* grid size, and for each effective grid position there is an input (IP) and output (OP) interrogation point. Here, if L and W are the length and width of the element in grid units, then IP and OP assume an integer value in the range $0 \rightarrow ((L \cdot W) - 1)$.

The code received at the baseboard includes information on the particular element's relative orientation to the interrogating element (or to the baseboard if it happens to be the lowest element in the structure), on the physical dimensions of the element being interrogated, and on the code for the input point (IP) at which it is being interrogated. The code for the output position (OP) currently being used on the interrogating element is calculated by processing the sequence of codes received as the baseboard interrogation proceeds.

The absolute position of the origin of the coordinates of any block is therefore determined by repeated application of the standard axes translation transform represented by

$$[x'\ y'\ z'\ 1] = [x\ y\ z\ 1] \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ T_x & T_y & T_z & 1 \end{bmatrix},$$

where x', y', and z' are the absolute coordinates of the element being interrogated, x, y, and z are the absolute coordinates of the interrogating element, and T_x, T_y, and T_z are defined by

$$[T_x\ T_y\ T_z] = \mathrm{OP} \cdot \mathbf{OR} \cdot \mathbf{A} + \mathrm{IP}' \cdot \mathbf{OR}' \cdot \mathbf{B} + \mathrm{H}' \cdot \mathbf{C},$$

Figure 8. Prototype two-unit element.

where OP is a scalar given by the code for the output position on the interrogating element, **OR** is a vector derived from the absolute orientation of the interrogating element, IP′ is a scalar given by the code for the input position on the interrogated element, **OR′** is a vector derived from the absolute orientation of the interrogated element, H′ is the height of the interrogated block in scale units, and **A**, **B**, and **C** are defined as follows:

$$\mathbf{A} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ -1 & 0 & 0 \\ 1 & -1 & 0 \end{bmatrix} \quad \mathbf{B} = \begin{bmatrix} -1 & 0 & 0 \\ 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix}$$

$$\mathbf{C} = [\,0 \;\; 0 \;\; 1\,].$$

This algorithm is readily programmed to allow the absolute positions of the defined origin to be obtained; from this information, the absolute position of the vertices of each element can be calculated using its physical dimensions and absolute orientation.

Prototype performance and use. The prototype system has been demonstrated successfully with a BBC Model B microcomputer (Figure 9) and a DEC Vax-11/750.[9,10] In particular, software, currently written in Basic for the BBC, translates the received data into a suitable database and performs the appropriate transforms to obtain the cartesian coordinates for the vertices of each element. To illustrate how this database may be accessed, we have written additional software to enable a perspective view of the structure to be displayed (Figure 10). Also, a simplified thermal analysis program[11] has been written to demonstrate how engineering evaluations can be applied to the database. This program assumes that the prototype blocks represent a room and allows the user to define the thermal properties of a particular block—for example, the percentage of glazing in each wall of the block and the thermal properties of the glazing and the fabric used in each wall. Using a typical yearly weather profile for the location of the building, the program can calculate the thermal gain or loss for the structure. An example of the output of this program is shown in the form of an isoplot in Figure 11. These examples illustrate that the database can be readily accessed by available applications software.

As far as we are aware no other three-dimensional input peripheral using our principle and having the capability demonstrated by our system is in existence. Frazer has presented similar ideas but his system does not appear to allow for structures such as lintels supported at two or more places.[12]

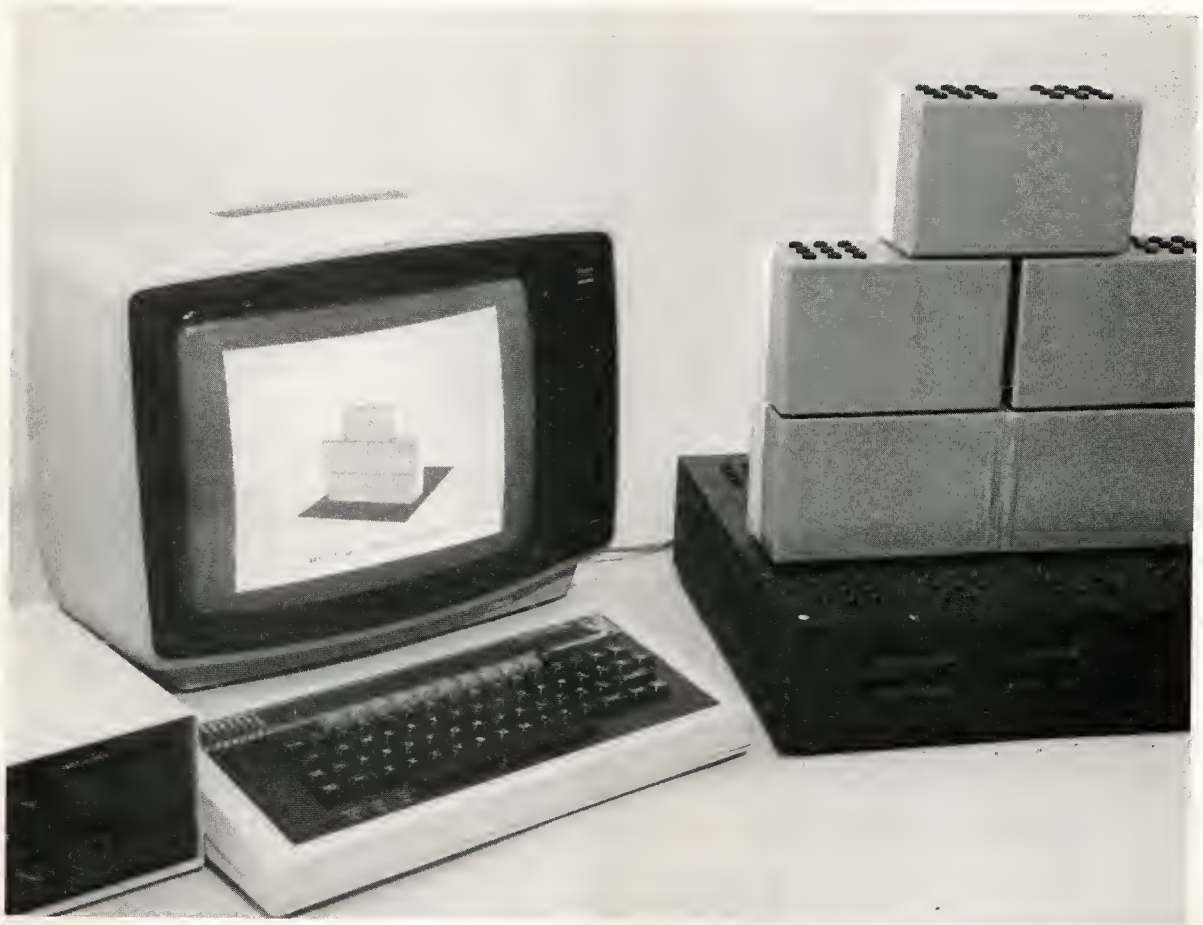


Figure 9. Prototype peripheral connected to a BBC Model B microcomputer.

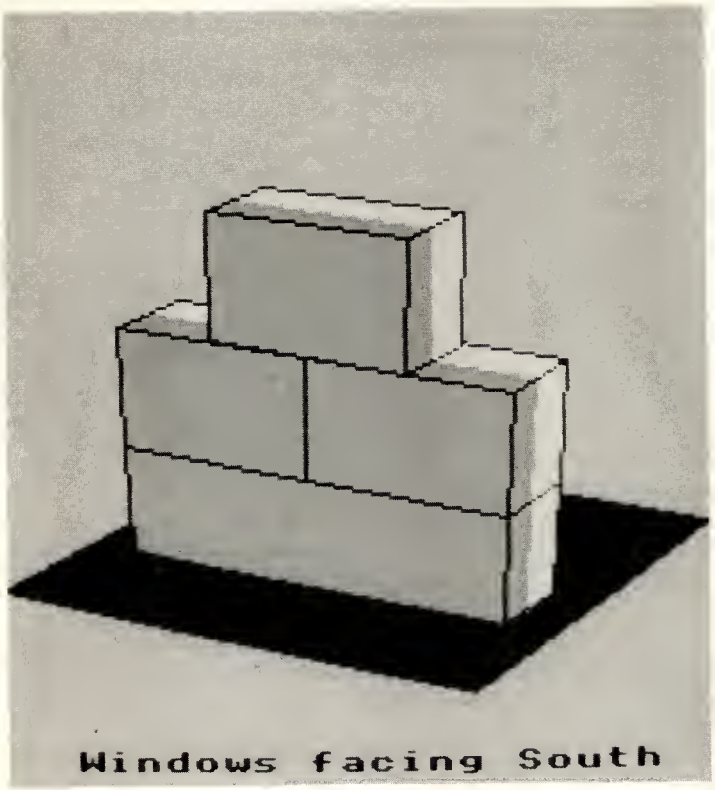


Figure 10. Perspective view of structure generated by the microcomputer.

The future

We are investigating a number of enhancements with the object of producing improved versions of the peripheral. The most important of these is the implementation of the element electronics as a single, low-cost integrated circuit. This is essential to the successful development of the peripheral. Such a circuit may take the form of a single-chip CMOS microcomputer programmed to implement the function of the element electronics, or it may be implemented as a single semicustom CMOS integrated circuit. Both solutions are under investigation. The former appears to offer a cheaper alternative, provided a suitable device and accompanying development system can be identified. The latter offers the advantage of direct implementation in a gate array such as the UK 5000. Early investigations suggest that this would be an initially expensive solution which would become cheaper as more devices were produced. However, whichever of these methods is used, it will allow the production of a more architecturally realistic modeling system incorporating a wider range of basic elements. The physical dimensions of the smallest of these elements are very dependent on the size of the integrated circuit and particularly on the number of inputs and outputs required. Currently a well-known, nonintelligent, commercial modeling system developed from a children's construction toy is used by over 200 organizations as an aid to

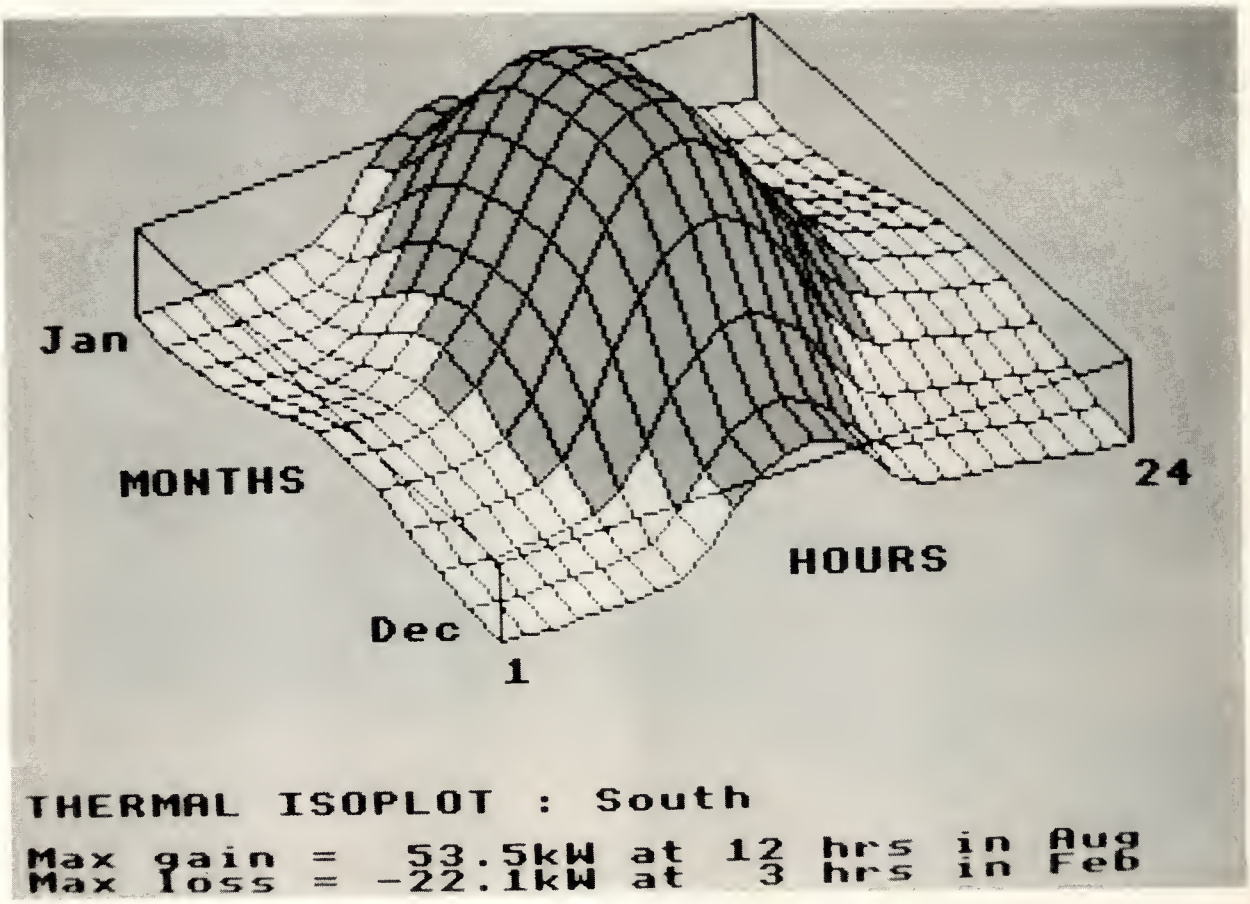


Figure 11. Thermal isoplot generated by the microcomputer for the structure in Figure 9.

the design of factory and process plant layouts and for town planning and architectural design. The smallest element in this system is 5 mm × 5 mm × 5 mm. We doubt that we can achieve this level of miniaturization in the next version of our peripheral, although we hope that we can produce a 1 cm × 1 cm × 1 cm element as the smallest unit. We envisage a baseboard nominally 64 cm × 64 cm together with a basic kit comprising some 1000 assorted building elements having physical dimensions which are multiples of the basic unit size.

The production of a more compact prototype will enable a more substantial evaluation of this new three-dimensional input peripheral as an effective man-machine interface, especially for computer-aided architectural design. The results of this work will be reported in due course.

Our prototype three-dimensional input peripheral is particularly suitable for use with computer-aided architectural design systems. However, this is not the only application we envisage. For example, our prototype could form the basis of a device to evaluate pattern or color matching in psychological testing or for molecular modeling. Also, given the increasing interest in home computing, it could serve as the basis of an educational toy combining children's interest in home computing with their interest in modeling. ■

Acknowledgments

The authors wish to acknowledge the financial support given to this project by the British Technology Group and the Ove Arup Partnership.

References

1. I.E. Sutherland, "Three-Dimensional Data Input by Tablet," *Proc. IEEE,* Vol. 62, No. 4, Apr. 1974, pp. 453-461.
2. H.C. Allison and D.P. Greenberg, "The Three-Dimensional Graphical Input Method for Architecture," *Proc. 15th Design Automation Conf.,* Las Vegas, NV, June 1978, pp. 133-137.
3. Data sheets, Science Accessories Corp., Southport, CT.
4. J.L. Posdamer, "Surface Geometry Acquisition Using a Binary-Coded Structured Illumination Technique," *Computers in Industry,* Vol. 3, No. 1-2, Mar.-June 1982, pp. 83-92.
5. UK patent specification no. GB 2 020 073A.
6. US patent specification no. US 4,275,449.
7. R. Aish, "3D Input for CAAD Systems," *Computer-Aided Design,* Vol. 11, No. 2, Mar. 1979, pp. 66-70.
8. C. Corbett, "G60 Bus Reference Manual" (internal document), Dept. of Electrical Engineering Science, University of Essex, Colchester, 1983.
9. R. Aish, "3D Modelling System for Computer Aided Architectural Design," *RIBA Conf.,* London, May 1984.
10. R. Aish and P.D. Noakes, "Architecture Without Numbers—CAAD Based on a 3D Modelling System," *Computer-Aided Design*, to appear, Nov. 1984.
11. R. Aish, "THERMAL—A Computer System for Building Services Design," *Proc. CAD 80,* Mar. 1980, pp. 627-640.
12. J. Frazer, "Intelligent Physical 3-Dimensional Modelling System," *Proc. Computer Graphics 80*, Brighton, UK, Aug. 1980 (Online Publications, London), pp. 359-370.

Peter D. Noakes is a lecturer in the Department of Electrical Engineering Science at the University of Essex in Colchester, England. His current interests are digital systems design, microprocessor applications, CAD on microcomputers, and signal processing. Noakes has a BSc (Eng) from Queen Mary College, London. Prior to becoming a lecturer in 1972, he worked for the Marconi Company in Chelmsford, Essex. He is a member of the IEE and is a chartered engineer.

Robert Aish is the manager of the Building Services Section of the Ove Arup Partnership Computer Group in London, England. His current interests include CAD software development for the thermal and visual analysis of buildings, interactive data handling and graphics systems, data acquisition techniques for monitoring solar heating devices, and 3D modeling systems for architectural design. Aish has a MDes from the School of Industrial Design (Engineering), Royal College of Art, London, and a PhD in man-machine systems from the University of Essex. Prior to joining Ove Arup, he was a research fellow with the Abacus Group at the University of Strathclyde, Glasgow. He is the author of the original patents for the interrogatable building block system. He is a member of the Design Research Society and of the European Association for Computer Graphics (Eurographics).

Questions about this article can be directed to Aish at 32 Chilbolten Avenue, Winchester SO22 5HD, UK; telephone (0962) 63087.

Adding a graphics tablet, a stylus, and special software to a personal computer system enables its users to edit text with simple, handwritten commands.

Word Processing with On-line Script Recognition

Wolfgang Doster and Richard Oed
AEG-Telefunken Research Institute

Up to now, the human way of writing down information, and of correcting and manipulating it, has been with pencil and paper. Electronic word processing equipment and its software, however, force the writer to get by the best he can with a keyboard. Instead of using the natural finger-stylus combination, he has to deal with the unnatural finger-key combination. The latest development in text processing software for personal computers is to offer a mouse for all pointing operations and a keyboard for text input only. However, it is in fact possible to route *all* the operator's commands, hints, and text inputs through the same input peripheral—a graphics tablet.

The graphics tablet, in combination with the appropriate software, can make human script viable as a means of computer input and offers the opportunity of making word processing, or, in general, the interaction between man and computer, really user-friendly.

Therefore, we devised a personal computer system organized around a digitizing tablet (Figure 1). After a program for the recognition of handwritten symbols, together with a small extension to the operating system, have been loaded, the user has a choice between two input possibilities:

- the standard keyboard or
- the tablet and stylus.

The tablet-stylus combination allows the input of commands, cursor control, and the input of characters. Therefore, the tablet-stylus combination, accompanied by suitable software, represents an extension of the mouse.

Here, we describe the principles of on-line script recognition and its application to word processing, and comment on its actual implementation and further development.

0272-1732/84/1000-0036$01.00

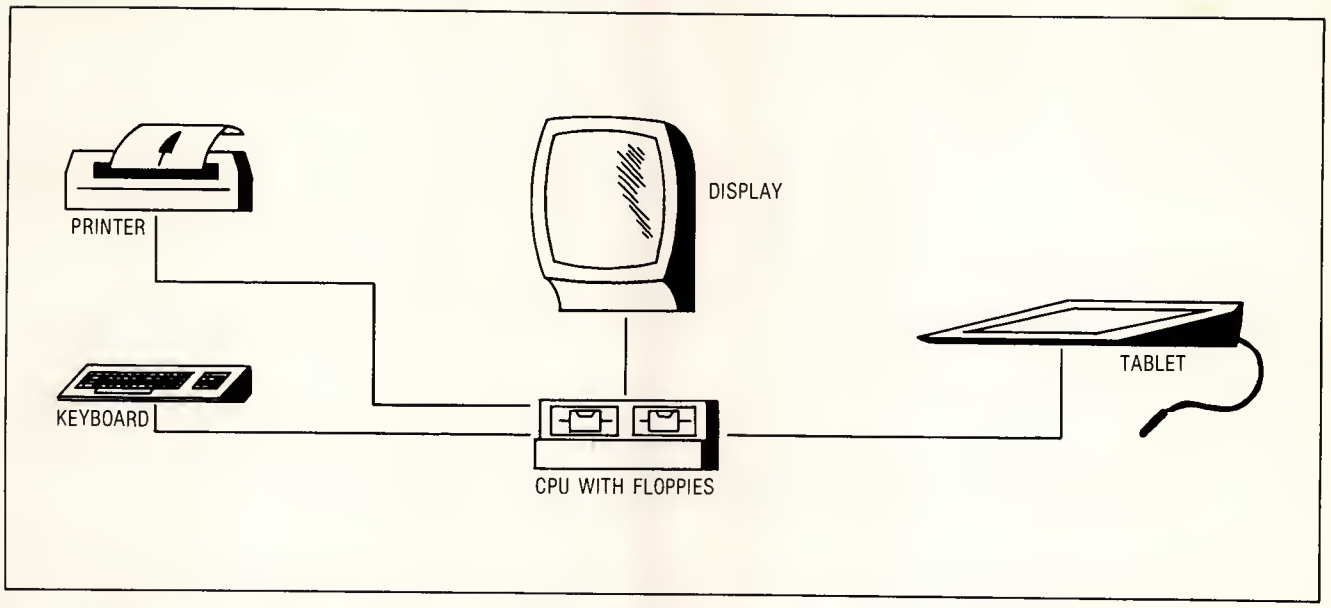


Figure 1. Our experimental personal computer. It includes standard peripherals and a graphics tablet.

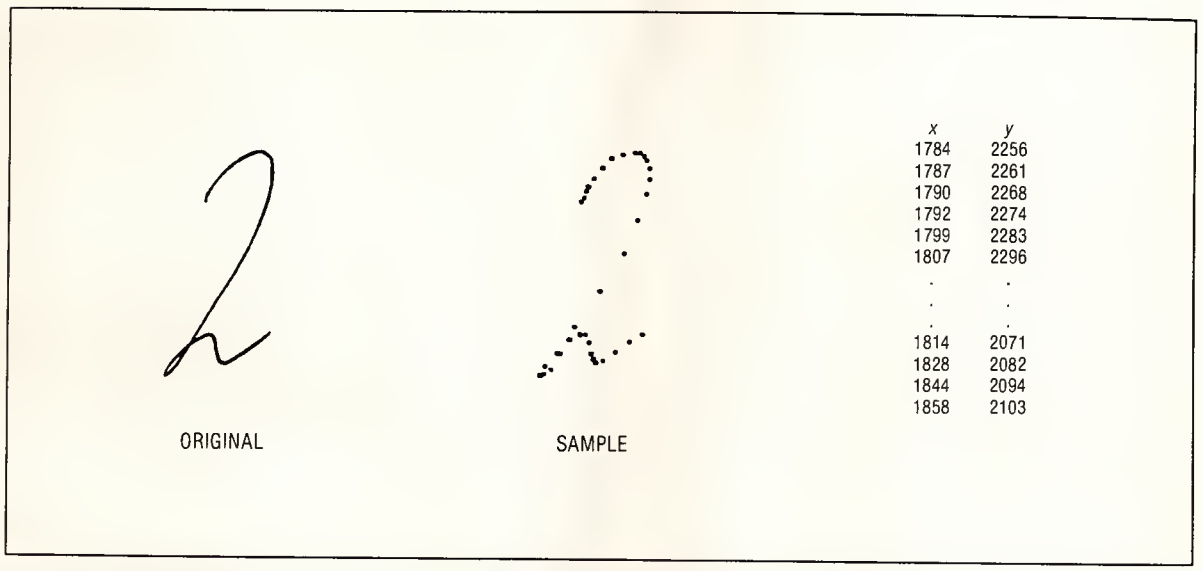


Figure 2. The character "2" in its original handwritten form (left), as sampled (center), and as represented by coordinate pairs (right).

On-line script recognition

The input data for on-line script recognition is collected by means of the graphics tablet. The tablet consists of the tablet itself and a stylus; both represent a transmitter/receiver combination. Tablets of this kind may be constructed according to various physical principles.[1] In our experimental system, we employed a magnetostrictive technique.

When the stylus approaches the tablet's surface, its coordinates are calculated by measuring the transition times of traveling magnetic wave fronts; the coordinate data are then transmitted to the computer via a V.24 interface. When the stylus actually makes contact with the tablet's surface, a switch inside the stylus is actuated to set a flag. During on-line script recognition, the flag is evaluated in order to segment connected line elements; for cursor control, the flag is used to fix the cursor to certain positions.

Tablet coordinates are passed to the interpretation program in the form of a continuous stream of coordinate pairs and flag bits. This sequence has to be segmented into substrings belonging to single characters (Figure 2). The next steps are size and time normalization and recognition. Interpretation of a string of coordinate pairs is initialized either automatically by time conditions or explicitly by activation of the "enter region" of a menu field. In any case, automatic interpretation starts if, after a predefined time period, no coordinates have been sent to the computer.

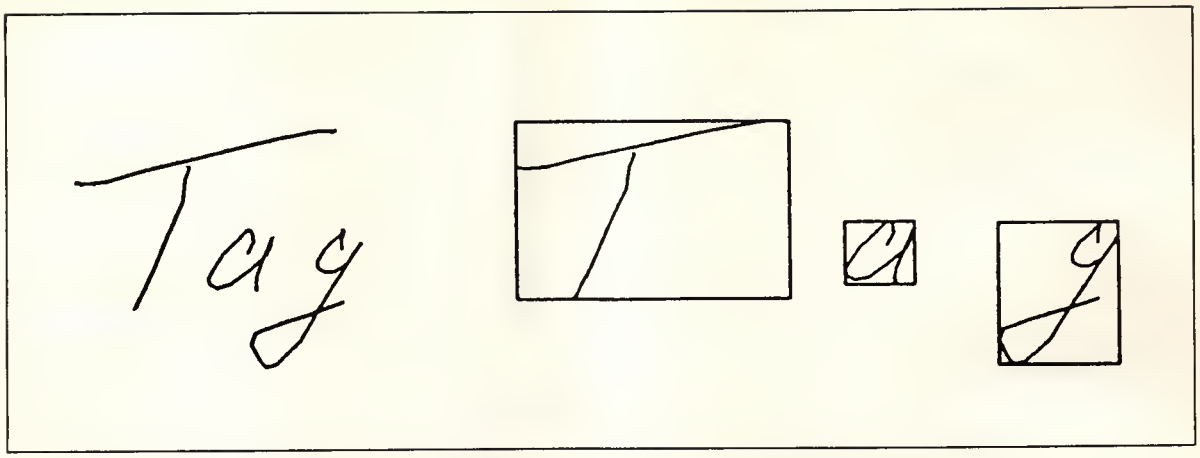


Figure 3. The character sequence "Tag" (left) and the result of its segmentation (right).

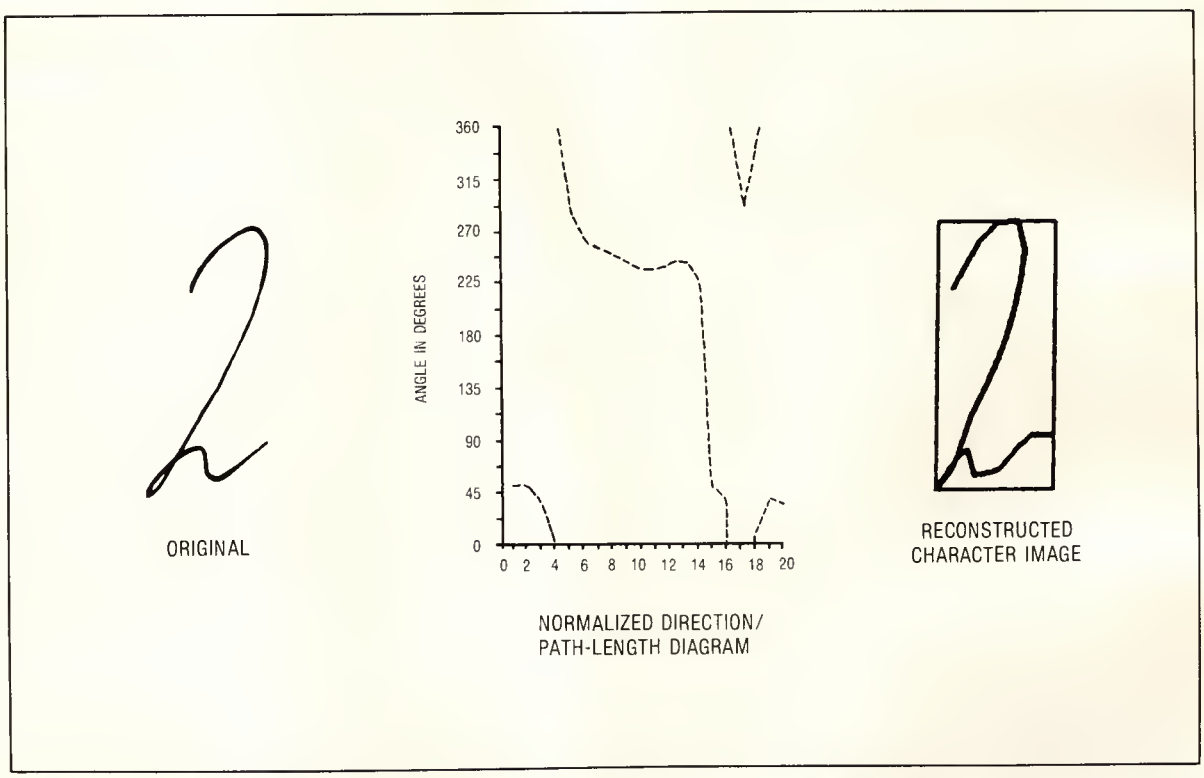


Figure 4. The character "2" in its original form (left), its normalized direction/path-length diagram (center), and its reconstructed image (right).

The string of coordinates generated while the stylus is in contact with the tablet is called a connected-line segment, or CLS. The number of CLSs may vary from character to character. There exist characters with one CLS, e.g., the digit "2", and characters with more than one CLS, e.g., the digit "4", which usually consists of two CLSs. A fundamental task, therefore, especially if a user writes more than one character at a time, is the grouping of the CLSs according to their corresponding character positions—that is, identifying which CLSs belong to one and the same character. This is called the segmentation process. A hierarchical segmentation procedure is applied. The first step is the selection of those subsets of the set of CLSs whose smallest surrounding rectangles are touching or overlapping. The second step is to check these subsets to determine whether they really belong together or not. Among the elements of the subsets, a direct distance measure between the corresponding CLSs is applied. Final segmentation is based on a predefined distance threshold. With this approach, even overlapping character sequences can be segmented correctly, as shown in Figure 3.

The scanning frequency of the tablet is constant. Therefore, writing slowly results in a higher number of coordinate pairs. Writing speed and symbol size must not influence the recognition result. To achieve this, all

connected-line segments are geometrically and dynamically normalized. The normalization directly corresponds to the construction of a direction-over-path-length diagram, with a suitably chosen predefined number of scanning points in the path length.

For each CLS, there is a corresponding smallest surrounding rectangle. Additionally, a common rectangle is constructed for characters with more than one CLS. The location of the subrectangles within the common rectangle yields additional features for recognition.

Figure 4 shows a character in its original form, its normalized direction/path-length diagram, and its reconstructed image. Here, the reconstruction is based on

- the angles given by the normalized character data,
- a unit path-length increment, and
- linear interpolation between the reconstructed coordinates.

A smoother version of the reconstructed image could be generated easily by using more sophisticated interpolation schemes.

After the processing described above is completed, the characters are classified according to a hierarchical branching procedure. The reference symbols are grouped into subsets depending on the number of CLSs in each character, and the first branching is done according to the number of CLSs actually measured. An input character is compared only to reference characters having an identical number of CLSs.

Presently, classification is realized through a euclidean-distance-measuring approach. Components of the distance measurement are the distances between the CLSs and the distances in the location of the smallest surrounding rectangles within the common rectangle. The results of the classification are measurements of identification reliability between the input character and each possible reference symbol (Figure 5). Depending on the measure of reliability, either an identification is outputted, or the decision is refused because the character cannot be reliably identified. It is possible, however, to have alternative identifications outputted, with the number of alternatives controlled by the measure of reliability.

Our experimental program for on-line script recognition also includes components for interpretation and presentation of intermediate results of the various processing steps, and components for editing the reference symbol set. Identification labels can be changed or erased, and new symbols can be added to the reference symbol set. The user can add his own "private" characters and symbols to the reference set—almost any user-defined handwritten symbol can be accommodated.

Combining on-line script recognition and word processing

We can distinguish two phases of word processing:

- creation of the text, and
- further manipulation (correction and editing) of the text).

In the following discussion, we consider only the second aspect, since on-line script recognition is probably too slow to use for text creation in commercial word processing environments. In such settings, initial creation of text is done with keyboards by persons accustomed to using keyboards. Even today (and much more so in the near future) text creation can take the form of direct document input via OCR devices.[2] And in the farther future, it will also be accomplished with connected-speech recognition systems—i.e., with voice-activated typewriters.

During the further processing of text after its initial creation, the input consists mainly of commands to the word processing program together with occasional characters—i.e., insertions or corrections. These user interactions—commands and character input—each take a characteristic form:

- commands are entered by means of separate function keys or control sequences;
- characters are entered via the standard keys of the keyboard.

On a personal computer with a word processing package such as Wordstar,[3] the operator interacts with the program via a screen menu such as that shown in Figure 6. Depending on the keyboard hardware, the operating system, and the specific word processing program, the operator, to give commands to the system, has to either strike function keys or type sequences of characters while depressing the CONTROL key. For cursor control, he must use either control sequences or the arrow keys (cursor control keys).

If the operating system of the PC has multitasking capabilities such as those offered by Concurrent CP/M-86,[4] the on-line script recognition software (with a graphics tablet) can be simply and elegantly combined with any other program. For this purpose, the keyboard buffer can be made to assume the central function of a mailbox for interprocess communication.

In such an arrangement, Task 1 is the word processing program, e.g., Wordstar, and Task 2 is the on-line script recognition program. The goal is to offer the user two parallel input channels: the keyboard and the tablet. To realize this, the on-line script recognition program, after recognizing one or more characters or symbols, has to write the corresponding sequence of characters into the keyboard buffer allocated to the other task (Wordstar). This sequence will imitate exactly any possible sequence entered through the keyboard. The keyboard-buffer-filling process carried out by Task 2 (on-line script recognition) is completely transparent to Task 1 (the application program, such as Wordstar). Figure 7 illustrates the interconnection of the two tasks by means of the keyboard buffer.

For word processing, commands, cursor movement, and text input must be distinguished from one another. This fact remains valid even if on-line script recognition is used.

In our system, cursor control seemed most suitably accomplished through the use of a separate cursor control

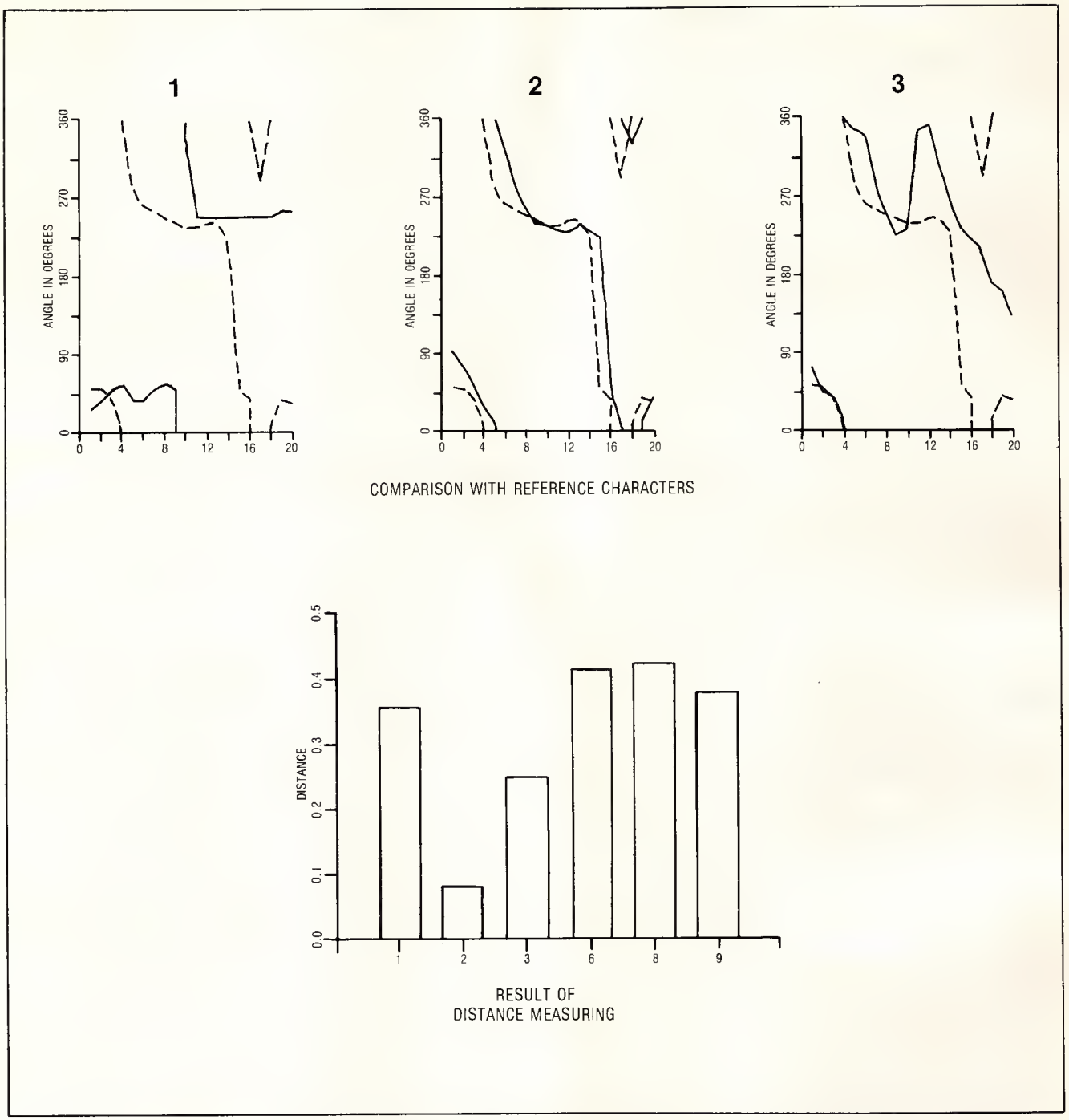


Figure 5. Comparison of the input character "2" with the reference characters "1", "2", and "3". The comparison yields the normalized direction/path-length diagrams shown at top. The dashed line in each diagram is for the input character; the solid line represents the reference character. The difference in distances (bottom) is clearly minimum for the reference character "2".

field on the tablet (Figure 8). Cursor control is activated as soon as the stylus approaches the surface of the cursor control area; tapping on the surface results in fixing the cursor at that point. A second tapping makes the cursor movable again. The cursor control area on the tablet is a scaled projection of the screen; a movement of the stylus over the cursor control area results in a corresponding movement of the cursor on the screen. The cursor control field operates with relative coordinates and has no fixed zero point. This makes the stylus and cursor control area comparable in function to a mouse. By setting different scalings of the cursor control area, the operator can change the relationship between the movement of the stylus and the movement of the cursor on the screen. The effect is slowed-down or speeded-up movement of the cursor, or scrolling.

After the cursor has been positioned, commands or text can be inputted. The word processing program operates

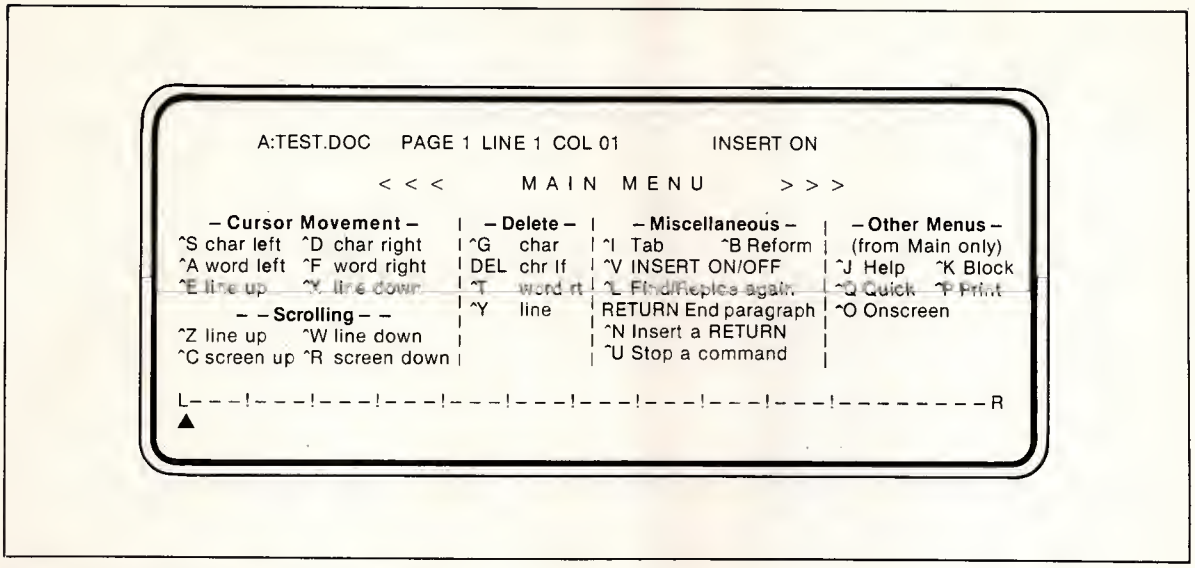


Figure 6. Example of a Wordstar menu.[5]

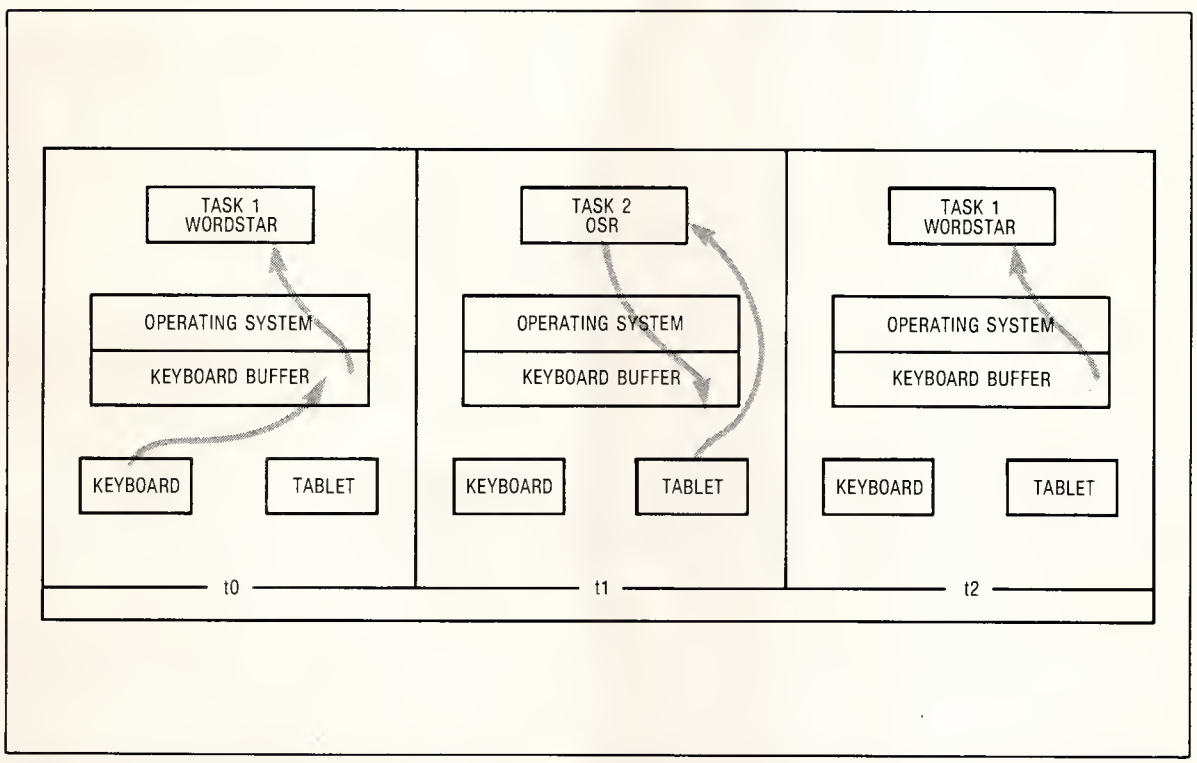


Figure 7. Interconnection of word processing (Task 1) and on-line script recognition (Task 2) by means of the keyboard buffer.

independently of on-line script recognition; this means, for example, that if the standard starting mode—the default mode—is insertion, then it remains the standard mode.

The tablet surface is partitioned into two major sections—the menu area (including the cursor control area) and the on-line script recognition area (or "active area"—see again Figure 8). The menu area is divided into separate fields. The first menu field is used for direct input of alphanumeric symbols. The second menu field enables entry of user-defined commands. The third field is the cursor control area.

For text input, besides the standard character set consisting of digits, lower- and uppercase characters, and special characters, additional symbols corresponding to RETURN (ENTER), DELETE, and CONTROL have to be defined. These symbols are also useful for command input—with them, the operator can write control se-

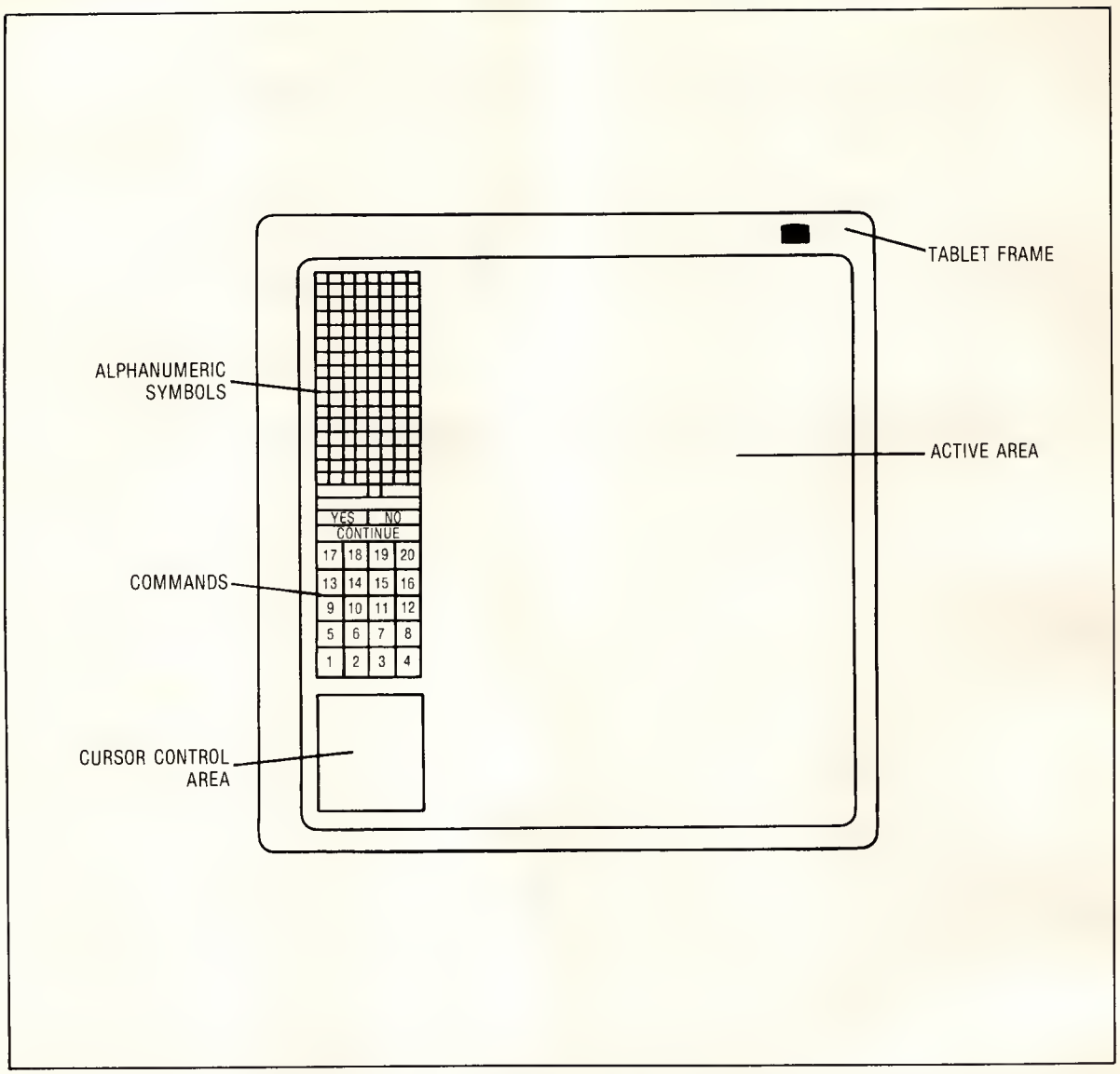


Figure 8. The digitizing tablet comprises two main sections—a menu area (left) and the on-line script recognition, or active, area (right). The menu area is further divided into separate fields for alphanumeric symbols, commands, and cursor control.

quences on the tablet instead of typing them on the keyboard. He can look at the screen and write them almost blindly on the tablet and they will be recognized, since the recognition process does not require input characters to be written in any particular place in the active area of the tablet.

However, the full potential of on-line script recognition cannot be realized unless the user employs the system's ability to define special symbols representing sequences of normal ASCII characters. For example, instead of writing the symbol for CONTROL and then the characters which follow it, the operator can define a special symbol to stand for the entire control sequence, and then write just that one special symbol.

In order to limit the number of reference characters to which comparisons have to be made, and thus to increase recognition accuracy, the set of reference characters is divided into two subsets. One set is the set of command symbols, and the other is the set of all standard characters and symbols. The latter is the default set; a switch to the command symbol set occurs as soon as a control character or any other user-defined character is recognized. After a sequence of characters has been written and interpreted, the recognition program automatically switches back to the standard character set.

In our system, the Wordstar application is displayed on the screen while the on-line script recognition program is running. The recognition program uses only the bottom line, where it displays messages—such as one notifying the operator that an input character has been rejected. However, if the operator writes a special switching symbol on the tablet, he can transfer the screen from the Wordstar application program to the on-line script recognition program (and vice versa). When the physical screen is at the recognition program's disposal, written and recognized symbols are directly presented on the

screen and not transferred to the keyboard buffer. This mode is used for testing on-line script recognition and for editing the reference character set (changing the labels, adding new reference characters, deleting old reference characters, and so on).

Our experimental on-line script recognition system was implemented on a 16-bit CPU with Pascal/MT+86, running under Concurrent CP/M-86. Its goal is to let an operator edit files without using a keyboard. The solution presented here—writing from one task into the keyboard buffer of another task, allowing the operator to define his own special symbols for commands and command sequences, and allowing him to input all characters in his own handwriting—represents a highly user-friendly approach to both text processing and other personal computer applications.

Further work will be concerned with user acceptance and with algorithmic improvements. We plan to test and improve our comparison and classification procedures so that a greater variety of characters can be recognized, with greater reliability. Our long-term goal is the recognition of slightly connected script and, after that, the recognition of connected script. ■

Acknowledgments

This article is based on a contribution to a workshop on interactive systems on personal computers held at Zürich, Switzerland, in March, 1984, and organized by a technical committee of the Gesellschaft für Informatik.

References

1. *Raster Graphics Handbook,* Conrac Division, Conrac Corp., Covina, CA, 1980.
2. W. Doster and J. Schürmann, "A Step Towards Intelligent Document Input to Computers," *Proc. Conf. on Computer Vision and Pattern Recognition,* Washington, DC, June 1983, pp. 515-516.
3. *Wordstar 3.0 User's Guide,* Micropro Int'l, San Rafael, CA, 1981.
4. *Concurrent CP/M-86,* Digital Research, Pacific Grove, CA, 1983.
5. A. Naiman, *Einführung in Wordstar,* Sybex Verlag GmbH, Düsseldorf, West Germany.

Wolfgang Doster joined the Pattern Recognition and Image Analysis Group of the AEG-Telefunken Research Institute, in Ulm, West Germany, in 1973. He has been involved in research relating to contextual postprocessing applied to postal address reading machines. His current research interests are in document analysis, on-line script recognition, and integration of these tools into office automation. Since 1980 he has also been teaching text communications at the Fachhochschule Ulm.

Doster received the Dipl.-Inform degree in 1973 and the Dr.rer.nat. degree in 1980, both in computer science from the University of Karlsruhe, West Germany. He is a member of GI—the Gesellschaft für Informatik, VDE/NTG, Eurographics, and the IEEE Computer Society.

Richard Oed is a member of the staff of the AEG-Telefunken Research Institute in Ulm. In 1981 he joined the Pattern Recognition and Image Analysis Group, after having worked for two years in the Radar Division. From 1979 to 1981 he was engaged in text-processing-related research, including introduction to text processing systems, training, extension, and documentation. His current interests include on-line script recognition, operating systems, personal computing, software ergonomics, and system integration.

Oed received the Dipl.-Ing. (FH) degree in 1979 from the Fachhochschule Ulm.

Questions about this article can be directed to the authors at AEG-Telefunken Communication Systems, Ulm Research Institute, Postfach 17 30, D-7900 Ulm, West Germany.

By incorporating on-chip signal preprocessing, this CMOS switched-capacitor-based A/D converter improves the speed and accuracy with which a microprocessor system can sense physical forces such as pressure and acceleration.

A Smart Digital-Readout Circuit for a Capacitive Microtransducer

Ernst Habekotté and Stefan Cserveny
Centre Electronique Horloger SA

Extremely rapid progress in silicon planar technology and in computer-aided design techniques has made signal processing circuits cheaper than ever before. Yet, the necessary input and output transducers still lack the level of maturity needed to fully exploit this progress. Input transducers are especially lagging behind. Here, we will present a CMOS switched-capacitor A/D converter for a capacitive microtransducer, with the necessary logic to control it. This converter and microtransducer, at present a two-chip solution, permit a microprocessor system to sense a physical quantity (such as mechanical force, electromagnetic force, acceleration, or pressure) in its surrounding nonelectric world.

The converter has been integrated in 6-μm micropower CMOS technology and covers approximately 3.6 mm^2. Since control logic for this converter was not included on the first test chip, breadboarded logic was used.

Background

The present state of the art in integrated circuits allows larger and more complete systems on one chip. One of the most impressive examples is the HP CPU, which integrates 450,000 transistors.[1] However, for many microprocessor applications, there is a barrier which lies

0272-1732/84/1000-0044$01.00

not in the microprocessor itself but in its periphery, in its communication with the surrounding nonelectric world.

Over the last few years, important progress has been made with batch-processed sensors in standard IC technologies. The main advantages of this approach are

- the potentially low fabrication cost (arising from batch fabrication),
- the small size achievable by accurate dimensional control (via microlithography), and
- the compatibility with on-chip signal processing circuitry.

Nowadays most sensors are passive elements that convert signal energy into electrical quantities. The transmission of this usually small electrical signal to the processing circuitry can be easily disturbed by electromagnetic interference. This problem can be overcome by smart transducers that combine sensors with active interface circuitry that performs the signal conditioning and preprocessing. This allows nonperturbed communication either with remote microprocessor systems or directly with actuators (e.g., displays).

The tendency in sensor development is therefore towards sensors with on-chip signal preprocessing. Several types of sensors (for example, temperature, magnetic, and optical) fit very well into the concept of a smart transducer, since the technology used for their fabrication is almost completely compatible with standard IC technology.

However, a lot of other sensors (for example, micromechanical and chemical ones) need special fabrication steps. In the case of micromechanical devices, special chemical etching techniques are used to form three dimensional structures—like diaphragms or cantilevers[2]—which have special sensing properties. Such sophisticated processing does not *directly* interfere with IC fabrication, but it does make the whole fabrication process much more complicated. For example, chemical etching can adversely affect the properties of the silicon substrate for the signal processing part of the device if special care is not taken.

Several sensors with not too complicated on-chip circuitry have already been realized.[3,4] In most cases, however, the first step in the direction of an intelligent transducer involves a two-chip solution in which the sensing device and the processor are fabricated on separate chips and packaged as a hybrid device. Thus, problems associated with complex fabrication can be avoided and both chips can still profit from the advantages of IC technology.

Here, we will present such a hybrid solution for a capacitive micromechanical transducer. The transducer employs a readout circuit to convert a capacitor ratio into a binary code which is linearly related to the applied physical quantity. This is not possible with conventional converters—they require that postprocessing be done because they can only measure capacitor values separately. Our switched-capacitor A/D converter, however, permits direct measurement of the wanted capacitor ratio.

The signal preprocessing section of our device, which was realized in a standard CMOS process, will be the main topic of this article. We will briefly discuss the sensor in order to define the specifications for the signal processing circuitry. We will also discuss the principle of measurement, as well as the integrated circuit implications of this principle. The converter output can be serial as well as parallel and is directly compatible with microprocessor systems.

Some logic is needed to control our A/D converter, and it is described in the next-to-last section of this article. In the last section, we present some measurements we obtained with a realized test chip.

Circuit specifications

The sensor is a capacitive microtransducer in which the deformation of a diaphragm by a force (such as a direct mechanical force, an electromagnetic force, pressure, or acceleration) is exploited. The sensor output is a capacitance value which varies as the distance D between the two electrodes of a measuring capacitor C_M varies due to the applied force. This measuring capacitor is realized between an electrode on the diaphragm and another electrode on a fixed glass mounting. Another capacitor, C_R, which stays constant, is used as reference. This reference capacitor has one electrode on the nondeformable part of the silicon substrate and one electrode on the glass mounting; the distance between these electrodes is the same as that between those of the measurement capacitor, without diaphragm deformation. The reference capacitor C_R has been set to have the value of C_M when no force is being applied to the diaphragm. Because C_R corresponds to the zero value of C_M, and C_M is sensitive to the physical quantity to be measured, the best sensitivity and linearity can be expected if $C_R/C_M - 1$ can be measured.

Both capacitors are expected to have a similar temperature dependence. Therefore, their ratio will have a negligible temperature coefficient. The parasitic capacitances present at both ends of these two capacitors, as shown explicitly in Figure 1, should not interfere with

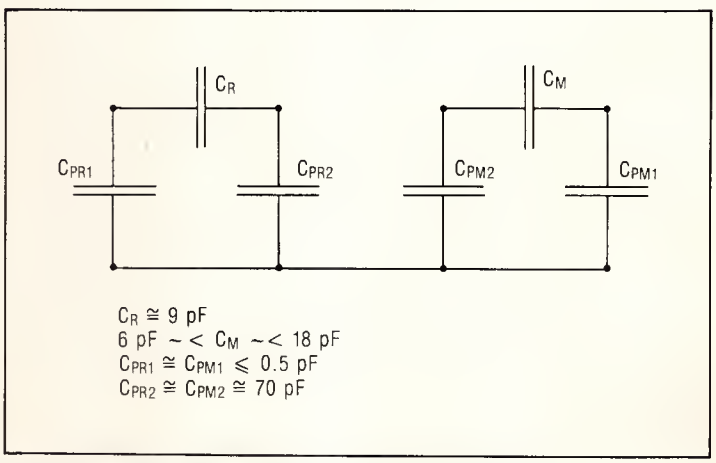


Figure 1. Electrical schematic of the microtransducer.

the measurement. The sensor can quite rapidly and precisely follow changes in the physical quantity. The objective of the interface circuit is to handle a frequency of up to 100 Hz with an accuracy of 0.1 percent, which means that the A/D converter has to have at least 10-bit accuracy:

$$1/2^{10} = 1/1024 \rightarrow 0.1 \text{ percent.}$$

The measuring capacitor C_M will not change more than 50 percent around its zero value.

Principle of measurement

Figure 2 shows a simplified electrical schematic of the converter. The flowchart in Figure 3 explains the measurement procedure. The converter, which has to measure the two capacitors C_M and C_R, uses them sequentially in the feedback loop of a high-gain differential transconductance amplifier[5]; a capacitor C and an array C_b (related to C) of selectable capacitors with binary-weighted values $C/2^n$ at the input of the amplifier allow binary-weighted charge transfers with C_M or C_R.

Each measurement begins with an *A/D converter initialization* through a total reset, i.e., a reset of the amplifier, of the comparator, of the input signal V_{IN}, and of the bits which control the array C_b (all capacitors $C/2^n$ connected to ground). Meanwhile, C_M is connected in the feedback loop. After the reset switch of the amplifier is opened, the first charge transfer with C_M in the feedback and only C at the input results in an amplifier output voltage of $-(C/C_M)V_{IN}$.

Memorization of this voltage in the coupling capacitor C_c is obtained by opening the reset switch of the comparator. The reset switch of the comparator stays open during the rest of the conversion. All the charge transfers which follow will be preceded by a *partial reset*, i.e., a reset of the amplifier and of the input signal. Thus, the effective input voltage for the comparator after each partial reset will be $(C/C_M)V_{IN}$. The result of the following charge transfers will be compared with this voltage. During the first partial reset, C_M will be replaced by C_R, which will remain in the feedback loop until the end of the conversion.

Sign detection is done with only C at the input ($C_B = 0$) and C_R in the feedback loop of the amplifier.

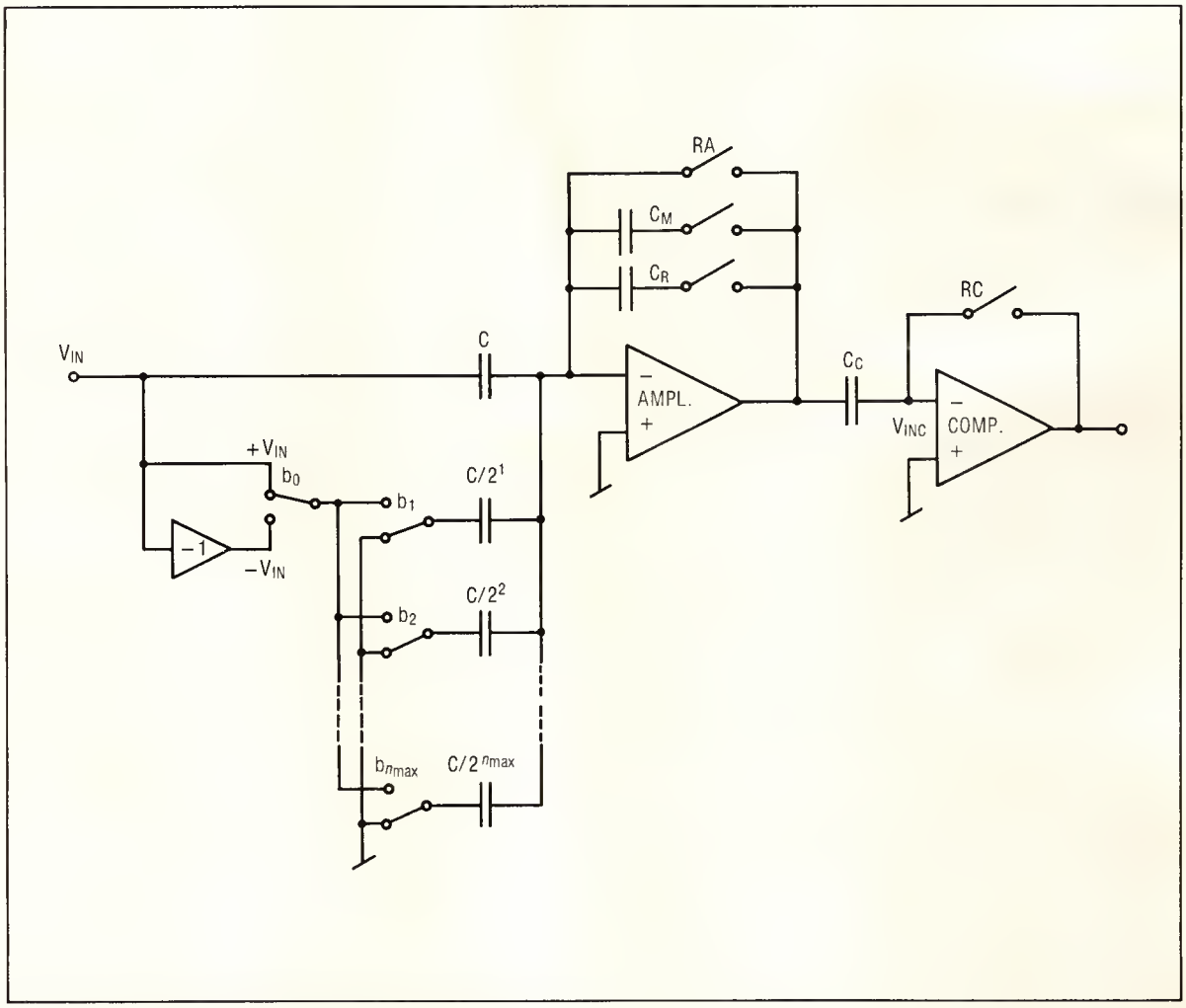


Figure 2. Simplified electrical schematic of the converter.

Thus, an output voltage $-(C/C_R)V_{IN}$ is created, resulting in a voltage difference

$$V_{INC} = C/C_R\ V_{IN}\ (C_R/C_M - 1) \quad (1)$$

at the input of the comparator. Now the sign decision can be made (sign bit b_0): a negative output from the comparator means that $(C_R/C_M - 1) > 0$, for which b_0 has to stay equal to 1; a positive output means that b_0 has to become 0. (Note that the comparator performs an inversion.) The switch controlled by bit b_0 allows selection of the polarity of the input voltage for the binary-weighted array as compared with the input voltage V_{IN} applied to C: $+V_{IN}$ if $b_0 = 0$. This defines a sign function:

$$\text{sign} = (-1)^{\bar{b}0} \quad (2)$$

Thus, the effective input capacitance values for the subsequent charge transfers are obtained by adding the sign times a binary-weighted capacitor to C.

First bit detection is done via a charge transfer with C + sign $C/2^1$ ($b_1 = 1$, $n = 1$) and C_R, which results in a voltage difference

$$V_{INC} = C/C_R\ V_{IN}\ [(C_R/C_M - 1) - \text{sign}\ 1/2^1] \quad (3)$$

at the input of the comparator.

Again, depending on the output of the comparator, it is possible to decide whether b_1 should be kept equal to 1 (sign $V_{INC} > 0$) or should return to zero (sign $V_{INC} < 0$). It is necessary to use (sign V_{INC}), since the logic has to make a decision about the output of the comparator depending on the sign function. (Note that before the sign decision, the sign has been initialized to be positive ($b_0 = 1$).)

For each subsequent bit, this cycle of resetting the amplifier and the input signal V_{IN}, obtaining the value of the charge transfer after C_B has been added to C while C_R stays in the feedback loop of the amplifier, and deciding whether the last added capacitor $C/2^n$ should be kept ($b_n = 1$) or left out ($b_n = 0$) can be repeated. Here, sign detection (b_0) and $C/2^n$) selection (b_n, $1 \leqslant n \leqslant n_{max}$) make it possible to realize a specific capacitor value defined as follows:

$$C_B = \text{sign} \sum_{n=1}^{n} b_n\ C/2^n \quad (4)$$

Generally, after every charge transfer, the voltage difference at the input of the comparator equals

$$V_{INC} = C/C_R\ V_{IN}\ [(C_R/C_M - 1) - C_B/C] \quad (5)$$

The output of the comparator corresponds to the inverted sign of this difference. Thus, with some logic to command the switches, the comparator can select the necessary bits (b_0 up to $b_{n_{max}}$, $n_{max} = 11$, in this case) to let the voltage difference (Equation 5) approach zero. Equation 5 shows that the binary code found for C_B/C approaches the analog value of $C_R/C_M - 1$).

Circuit implementation on a test chip

In order to verify the measurement procedure described above, we implemented a test chip containing only the A/D converter. The electrical scheme of this test chip is shown in Figure 4. The circuit-level implications of the measurement procedure are manifold, and are discussed below.

Input signal. The input signal V_{IN} (see again Figure 2) is introduced via input switches, by switching between the

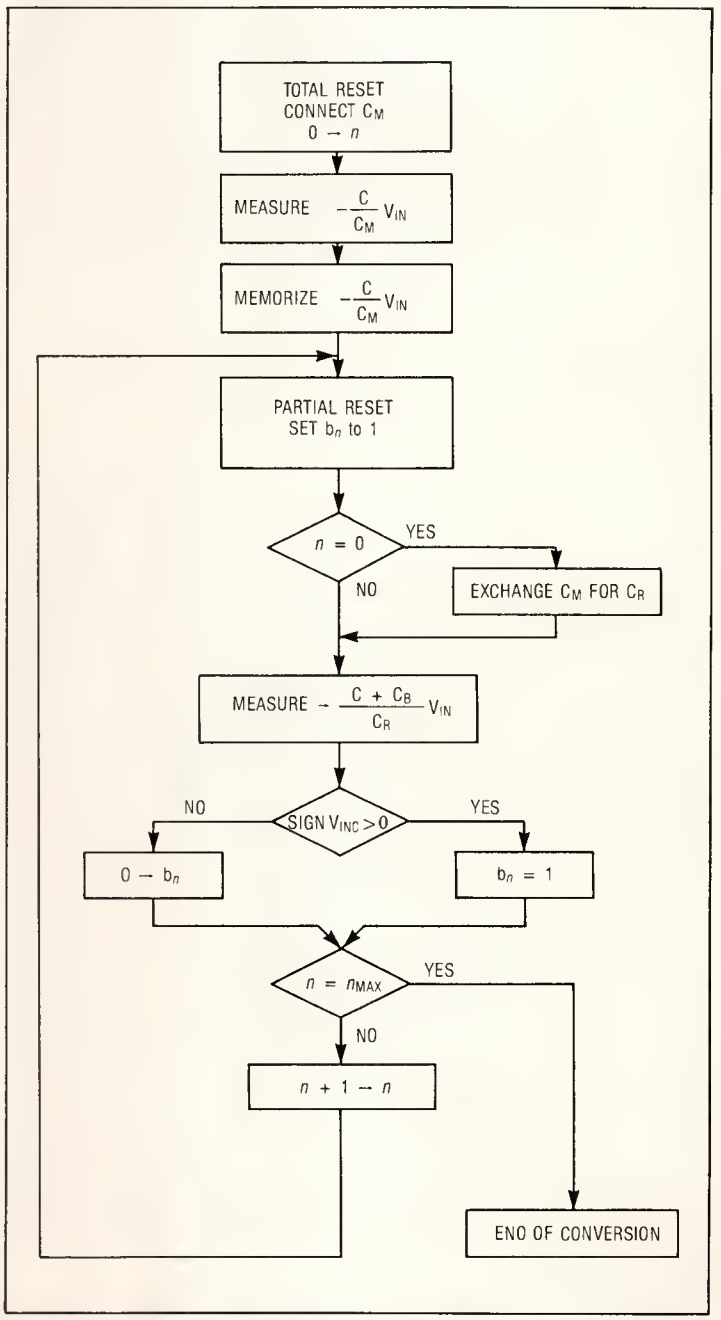


Figure 3. Flowchart of the measurement procedure.

two terminals VR+ and VR− of a reference V_{REF}, typically a bandgap reference ≅1.2 V (see again Figure 4). These switches also take care of the inversion of V_{IN} needed to define the correct sign for C_B/C, according to the inversion already available from the 1/32 attenuator (ATT in Figure 4).

Excessive parasitic capacitance. Because excessive parasitic capacitances related to one electrode of each sensor capacitor (C_{PM2} and C_{PR2} in Figure 1) can delay the converter too much, this electrode (from C_M for C_{PM2} and C_R for C_{PR2}) has been connected to the input of the amplifier. Here, however, a large parasitic capacitance could introduce an important error in the output signal. If the open-loop gain of the amplifier is high enough (> 95 dB), the parasitic capacitance of 140 pF can, in the worst case, introduce an error of 0.5 percent. Although we expected the amplifier to have an open-loop gain of approximately 90 dB, we included a source follower on the test chip. It can be used to guard against high parasitic capacitance related to a sensor-capacitor electrode when the open-loop gain of the amplifier is actually smaller than expected. The equivalent noise produced by this follower at the output of the amplifier is estimated to be less than 150 μV rms. (Note that the large parasitic capacitance of 140 pF with the smallest value for C_M introduces a gain of 140/6.)

Binary-weighted capacitor array. Because C_M will never change more than 50 percent in the sensor, $C/2$ ($n = 1$) has been left out. In order to demonstrate the ten desired bits, we added an eleventh bit to the converter. Eleven-bit accuracy implies that the smallest capacitor in the binary-weighted array has to be $C/2^{11}$. The largest capacitor C in the array should be kept close to the smallest value of the measurement capacitor C_M (≅ 6 pF) in order to avoid complete saturation of the amplifier when C_M is at its smallest value. This means that the capacitor corresponding to the least significant bit should be approximately 3 fF, which is not feasible with today's IC technologies. The smallest capacitor with matching properties good enough for 11-bit accuracy is approximately 100 fF.

Therefore, we introduced a 1/32 attenuator for $\pm V_{REF}$. Thus, some of the binary-weighted capacitors in the array allow a charge transfer with 1/32 V_{REF} at the input. For the corresponding binary-weighted charges at the input of the amplifier, these capacitors can be 32 times larger than in an array without the attenuator. This permits an array of binary-weighted capacitors in which

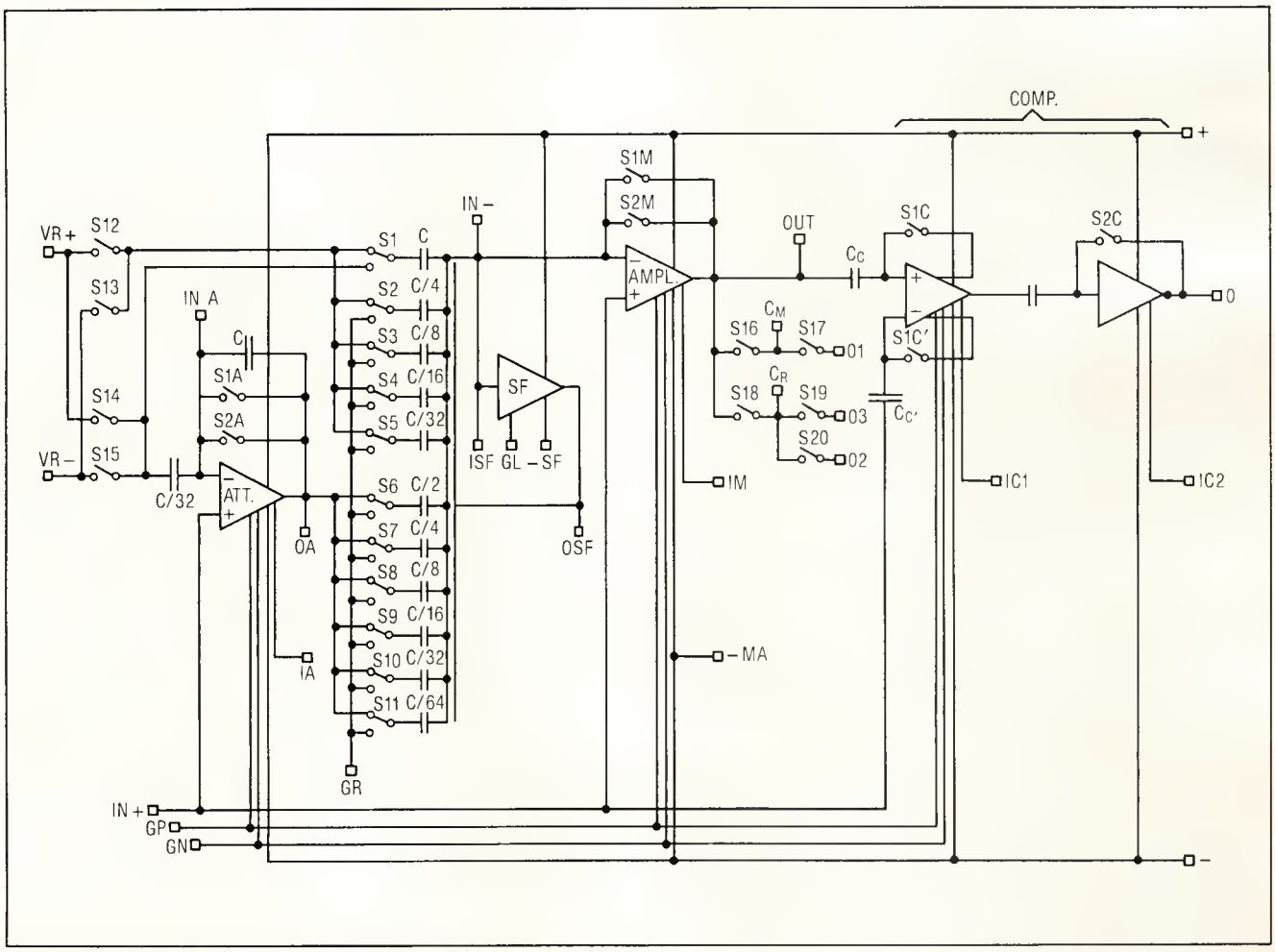


Figure 4. Electrical schematic of the test chip.

several capacitor values are used twice. The array uses the smallest capacitor of 100 fF as a unit cell. This unit cell is repeated as many times as needed to realize the other binary-weighted capacitors. These cells are disposed symmetrically around a central point.

The noise introduced by the amplifier in the attenuator ($\cong$ 150 μV, rms) limits the accuracy of the attenuator to 8 bits (150 $\mu V/(1/32)V_{REF} \cong 1/250$). This implies that not more than 7 least significant bits may be connected to the output of the attenuator. The attenuator is reset at the same time as the main amplifier.

Amplifier. The main amplifier must be capable of driving the relatively large sensor capacitors. Therefore, an adaptive biasing transconductance amplifier[5] has been chosen for this application. In this type of amplifier, the bias current is made signal-dependent; hence, the slew rate is much better than that in conventional designs, which have a constant bias current. Although the offset is not that important, since the amplifiers (main amplifier and attenuator) are separated by coupling capacitors and the offset is memorized in these capacitors, care has been taken to realize a low offset ($\cong$ 6 mV). Low noise is obligatory because, as already indicated, too much noise can ruin the attainable accuracy.

Clock feed-through error compensation. It is also because of the relatively large sensor capacitors that special attention was paid to the design of the reset switches. Reset time directly determines conversion speed; to obtain short reset times (several microseconds), it is necessary to use two relatively large complementary MOS transistors as a switch (a parallel circuit of P- and N-channel MOS transistors with $W/L \cong 54\ \mu m/6\ \mu m$). This, however, introduces a relatively large error voltage (several millivolts) due to clock feed-through (large overlap capacitances and channel-charge injection). If the value of the capacitor in the feedback loop stays the same during the conversion, this error voltage can be considered an offset voltage and can be memorized in the coupling capacitors. This can be done with the attenuator by opening its reset switch several microseconds before opening the reset switch of the main amplifier. However, replacing C_R for C_M in the feedback loop of the main amplifier can result in a noncompensated error, since C_R and C_M can have different values, though not ones more than 50 percent of the original error voltage. For 11-bit accuracy, the total equivalent error voltage has to be smaller than 500 μV. As the total noise comes close to 260 μV rms, the error voltage due to clock feed-through must stay below 240 μV. In order to achieve this, a smaller one-transistor switch (smaller overlap capacitances and smaller channel charge) is kept conductive to maintain the reset state after the larger reset switch has been opened.

Thus, only the opening of the smaller switch will introduce an error voltage—of approximately 1 mV and therefore of less than 500 μV for the maximum difference between C_M and C_R.

To reduce this error voltage further, a transistor with a short-circuited source and drain at the inverting input of the main amplifier can be made conductive directly after the smaller reset switch has been made nonconductive. In this way, this extra transistor with half the width of the smaller reset transistor will, by forming its channel, accept the charge injected by the reset switch.[6] Although it is difficult to predict how good this compensation technique will work out, it can be expected that with a relatively small fall time for the reset signal, at least 50 percent of the injected charge will be compensated for (i.e., a final error smaller than 50 percent of 500 μV will be produced).

Comparator. The comparator, which is very important in defining the accuracy of the whole converter, uses a differential input with a reset switch for each input, which is followed by an extra inverter stage with its own reset switch. The coupling capacitor between the differential stage and the output inverter allows memorization of the offset and of the response to the clock feed-through from the first stage by opening the reset switches in the differential stage before opening the reset switch in the second stage. Further, the clock feed-through in the differential stage will be effective at both inputs so that the common-mode rejection of the differential input can largely reduce the negative effect of the clock feed-through[7].

Converter accuracy. The accuracy of the whole converter is in fact limited to 11 to 12 bits, since the best matching properties possible with binary-weighted capacitors is somewhere between 0.1 percent and 0.5 percent.[8] The total noise in the worst case, estimated to be 260 μV rms, will make the twelfth bit uncertain ($260\ \mu V/V_{REF} \cong 1/4000 \cong 1/12$).

Figure 5 is a photomicrograph of the test chip, which covers approximately 3.6 mm^2 in a 6-μm micropower CMOS technology similar to the technology described by Vittoz, Gerber, and Leuenberger.[9]

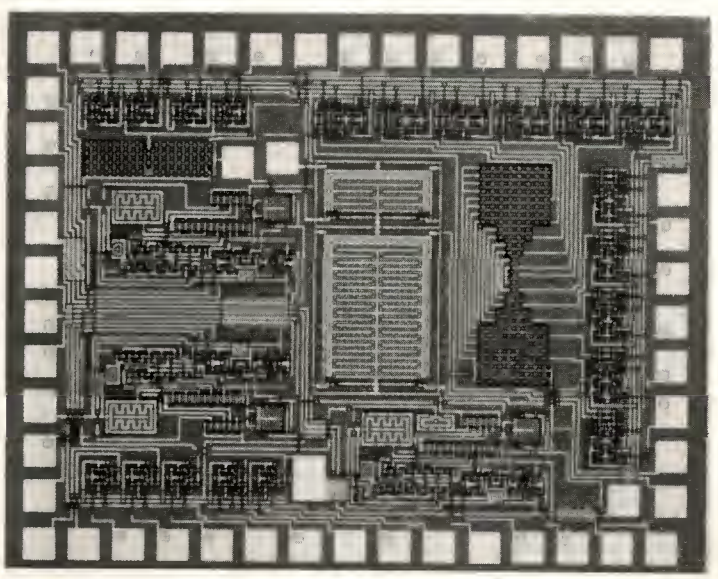


Figure 5. Photomicrograph of the test chip.

Command logic

A microprocessor could directly control the switches in the converter using the measurement procedure given in the flowchart shown in Figure 3. However, this would be complicated, since there are many control signals (25) besides the comparator output. Furthermore, this microprocessor would spend a lot of its available time controlling the A/D converter. It is much better to integrate the dedicated control logic with the A/D converter. This less-sophisticated logic controls the switches in the A/D converter according to the measurement sequence shown in Figure 3. It produces as either a serial or parallel output the obtained binary code, and it also takes care of the communication protocol (handshake) with the microprocessor system. This logic has been designed with $V_{IN} = -V_{REF}$. A simplified diagram of this logic is given in Figure 6. A counter controlled by the pulses from a clock generator defines through a decoder the timing sequence needed for all the switches in the converter.

The output of the comparator passes an input buffer containing a latch clocked by the decoder and a sign selection switch (sign V_{INC}) controlled by the sign bit b_0. Thus, the decision whether to keep or to drop the bit b_n after every charge transfer with the corresponding capacitor $C/2^n$ in the array can be taken. This is done as soon as the next charge transfer with $C/2^{n+1}$ (b_{n+1}) is able to be prepared during the reset of the amplifier (Figure 7). In this way, the output of the comparator controls the clear signal of every latch commanding the switches in the array. In the same way, the comparator controls the correct clocking of the input switches so that the reference voltage is introduced into the converter with the right sign (Figure 8). The correct sequence—i.e., first charge transfer with C_M, sign definition (b_0), and the 10 following charge transfers with C_R—is defined by the decoder and the counter. Each charge transfer lasts 16 pulses of the incoming clock in order to get the correct timing of the control signals. An extra counter running at 1/16 of the main elock is used to detect the end of conversion, when the chosen number of bits n_{max} has been reached. The conversion is concluded by putting the obtained binary code into the output buffer, by sending a ready signal to the microprocessor, and by thereafter sending the clear signal to the blocks inside the logic in

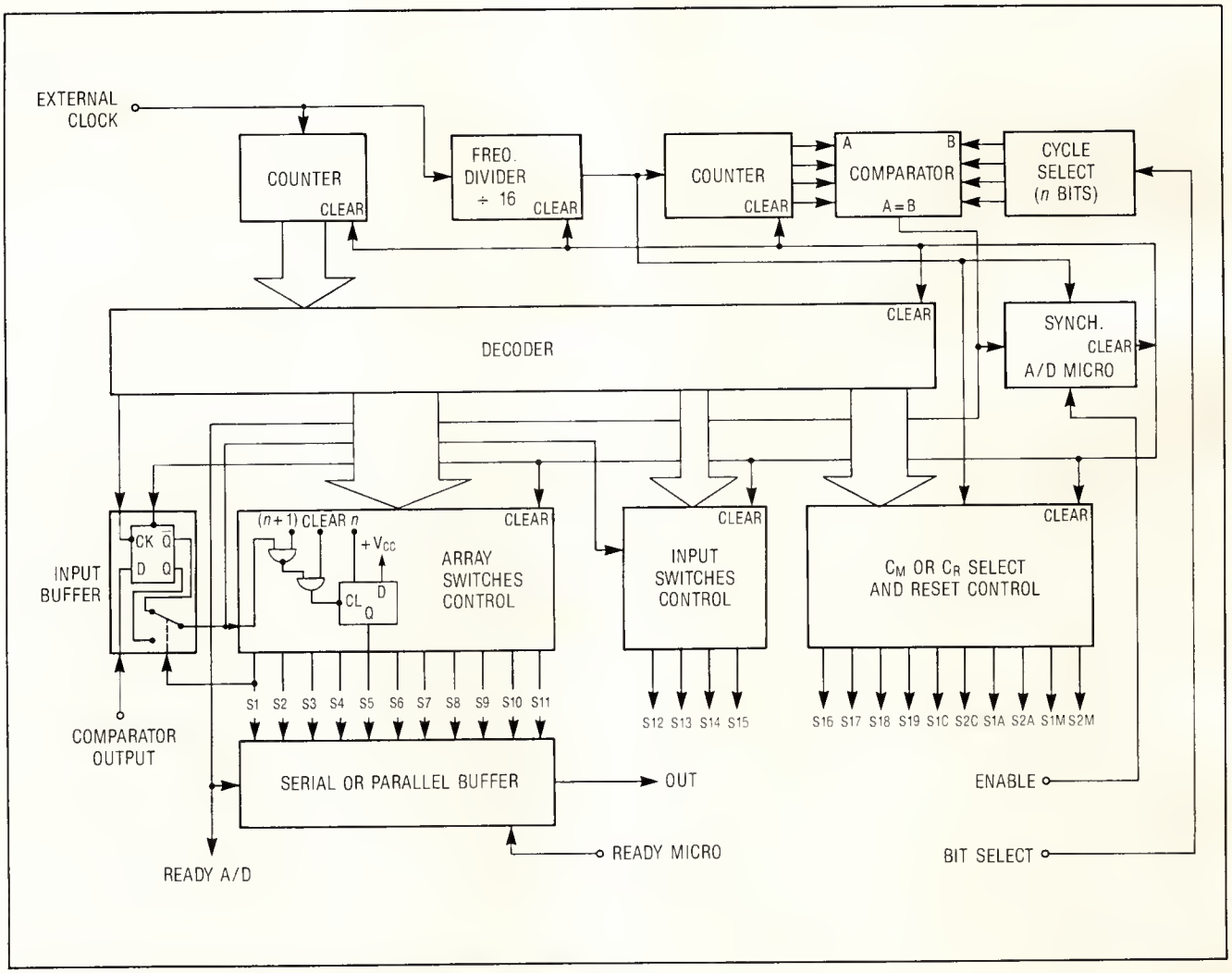


Figure 6. Schematic diagram of the breadboarded command logic.

order to reinitialize the converter for the next measurement (Figure 9). The ability to select n_{max} allows less precise but faster A/D conversion and, if a relatively fast change in C_M has to be followed, provides the necessary conversion speed to do so. With our logic, the converter continuously converts the analog value of the measurement as long as enable stays high. As soon as the microprocessor has received the ready-A/D signal, it can activate the output buffer with the ready-micro signal in order to get the last obtained binary code. The type of output buffer chosen depends on whether a serial or parallel output is desired. Although the logic could have been integrated on the same chip as the converter, it was not, for the reasons discussed at the beginning of this article.

Measurement

As it was not yet possible to measure a hybrid combination of the converter and the sensor, the problem of how to measure the test chip came up. External breadboarded circuitry, as shown in Figure 6, is used for the command logic in our experiments. For the purposes of measurement, the input of the main amplifier must be connected with one of the pins of the 64-pin, dual-in-line package used for the test chip. This, however, allows command signals from the logic to disturb the very sensitive input of the main amplifier through capacitance coupling. Clock signals with a voltage swing of four volts can create output signals of several tenths of a millivolt (precision of the converter less than five bits) through parasitic capacitances of only a few tenths of a femtofarad. Direct coupling between two pins is on the order of two picofarads! Another problem is how to create capacitor ratios which allow the measurement of small values of $C_R/C_M - 1$ in order to check the least significant bits. Using capacitors much larger than those in the sensor is not possible, since the main amplifier will introduce too much attenuation, which will prohibit measurement with the necessary precision.

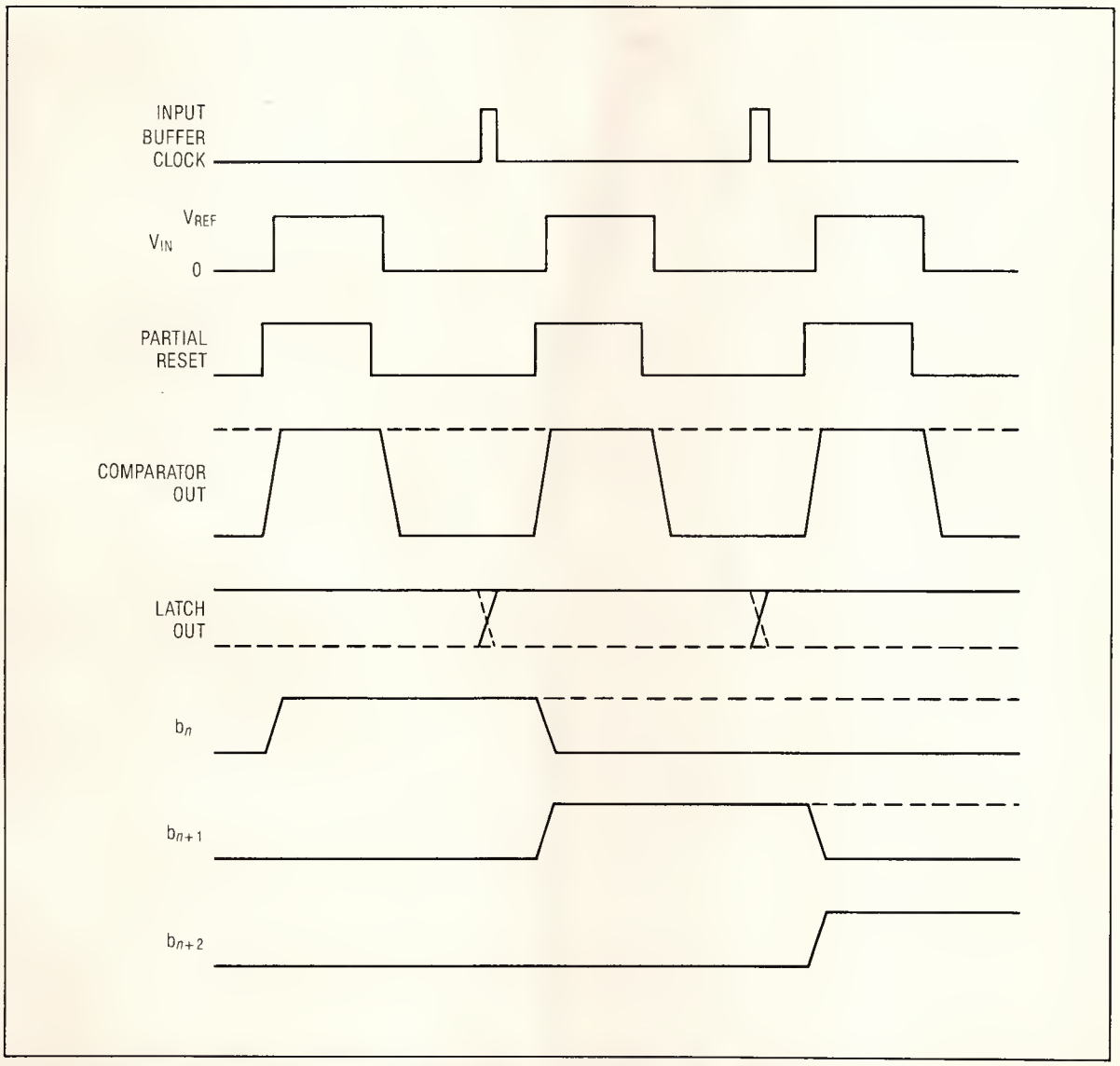


Figure 7. Bit select (and decision either to keep it high or to let it return to zero [sign bit $b_0 = 1$]).

Therefore, in order to get reliable measurements, the binary-weighted capacitor array of a second chip is used to replace the sensor capacitors. Thus, it is possible to avoid an external connection to the input of the main amplifier by mounting the two chips in one package. Because the smallest capacitor in the array is 100 fF (C/64), the measurements could have been limited to the sixth bit. However, with this solution, the converter can convert with its full precision.

A test measurement, with $C_M = C$ and $C_R = C + C/64$, is shown in Figure 10. In the upper part, the output of the main amplifier is depicted. The lower part shows the final result from the comparator; high output corresponds to the bits to be retained (plus the sign and the sixth bit). For this measurement, an extra amplifier (two inverters) was connected to the output of the comparator. This is why the reset phase for the comparator is not more apparent in Figure 10.

The smallest conversion time was approximately one-third of a millisecond (a longer conversion time is shown in the example in Figure 10). The test chip consumes about 300 μA at 4 volts, without the source follower, for a conversion time of 2.5 ms. In our 4-μm CMOS technology, approximately two times higher speed and a smaller chip area can be expected.

Our high-precision micropower CMOS switched-capacitor converter for a capacitive microtransducer offers several advantages. It outputs a digital code (11 bits plus sign) linearly related to the measured physical

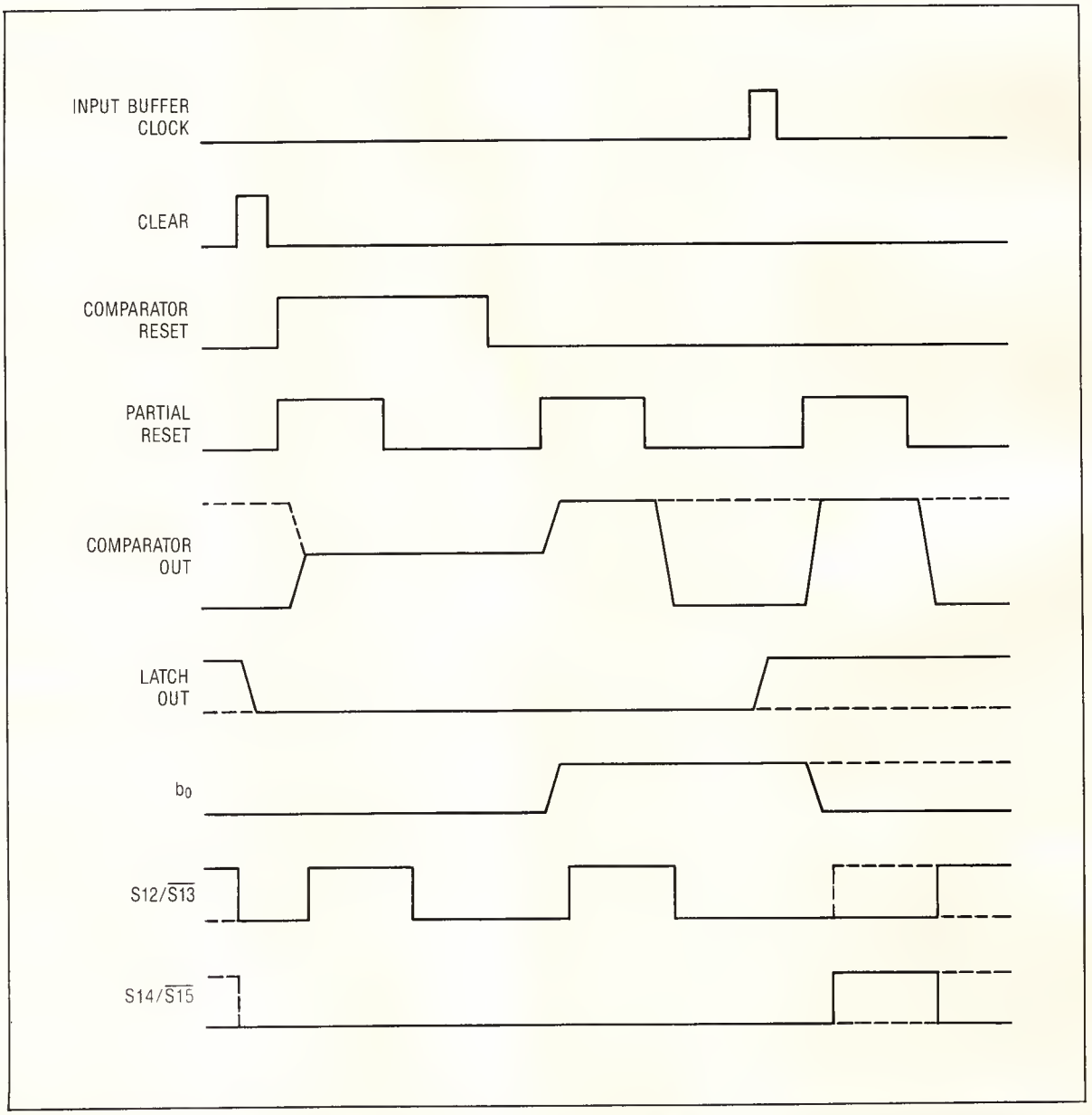


Figure 8. Input switch control at the beginning of the conversion (note that $V_{IN} = -V_{REF}$ for the first two charge transfers).

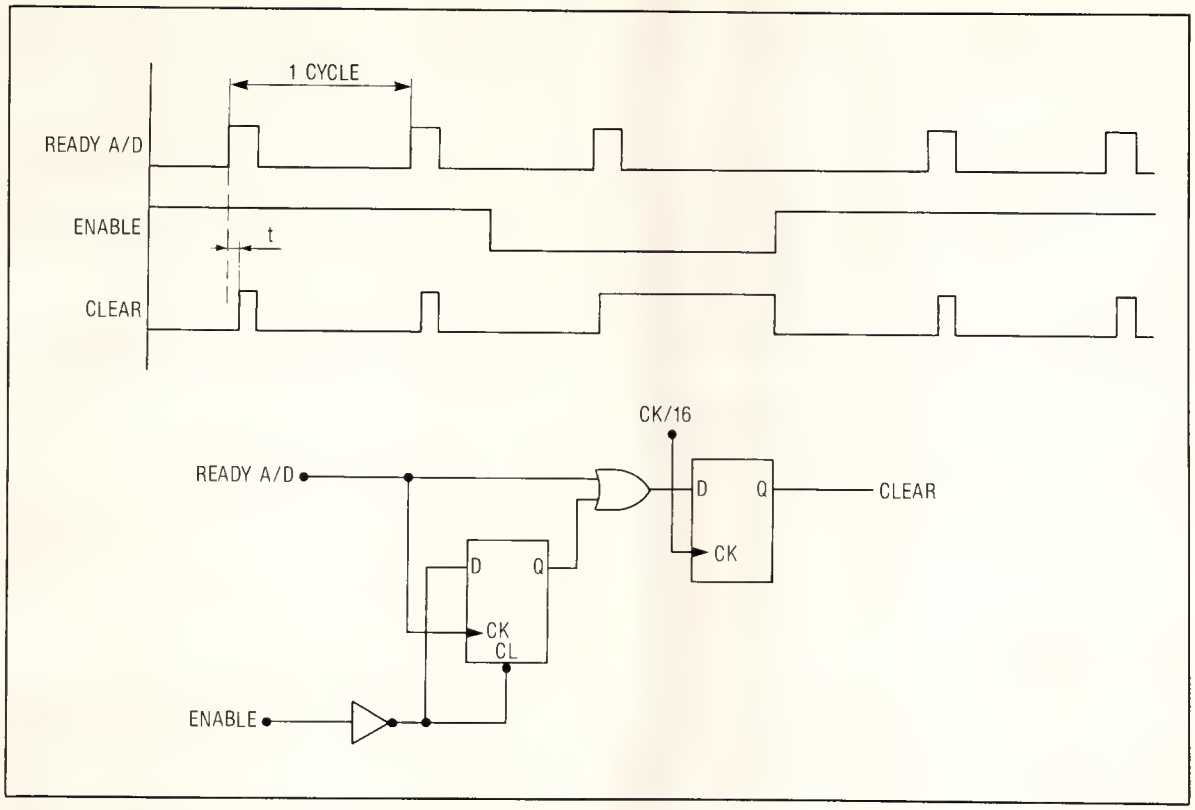


Figure 9. The end-of-conversion cycle.

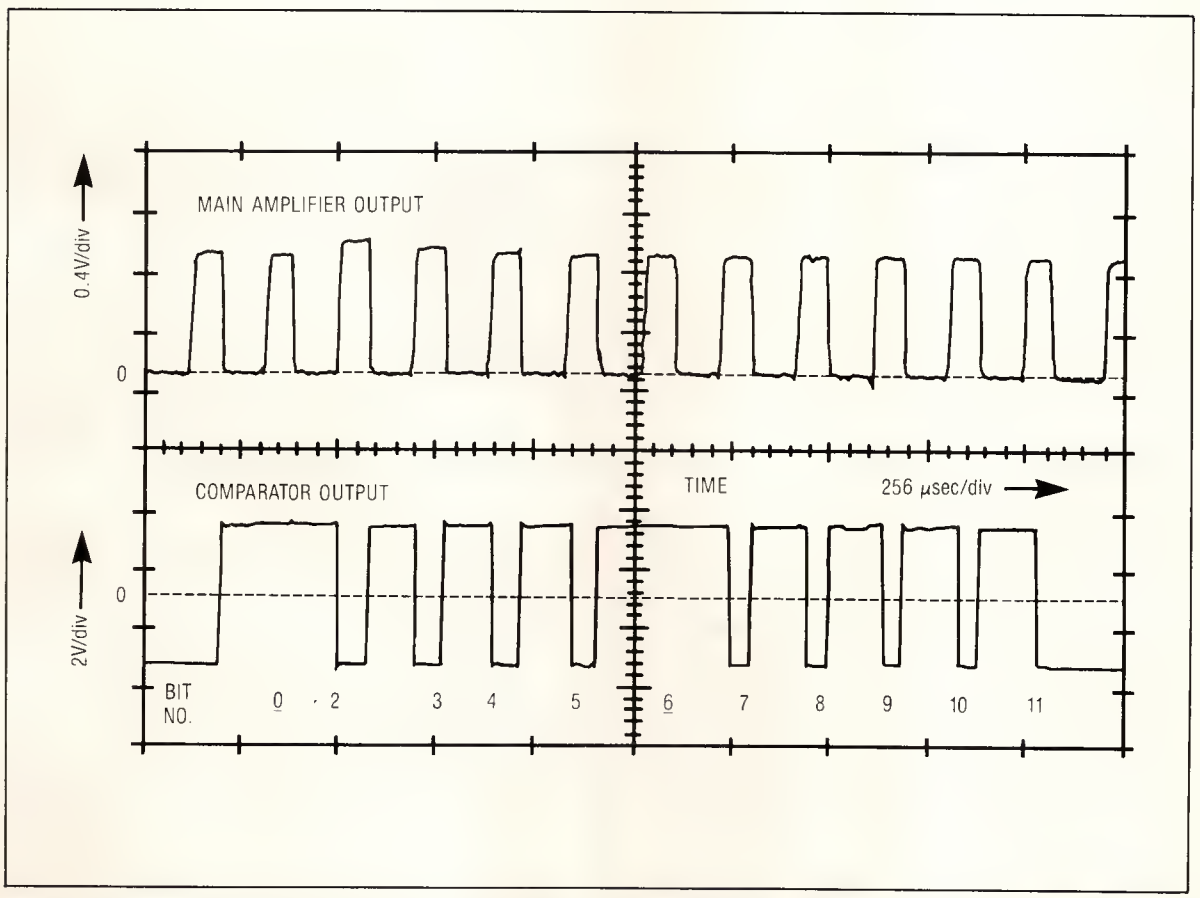


Figure 10. Measurement result with $C_M = C$ and $C_R = C + C/64$ (corresponding bit code for $C_R/C_M) - 1$ is +0000100000).

quantity within a 1/3-ms conversion time. The conversion time obtained allows the device to follow variations in the measurement-capacitor value of several hundreds of Hz. The measurement method does not require a precise voltage reference. (The only requirement is that the voltage stay stable during one conversion.) The correlated sampling provided by this method makes the converter insensitive to correlated or slowly varying perturbations (e.g., offset, most of the clock feed-through, 1/f noise, temperature). The method reduces the temperature sensitivity of the converter even further, since it compares a capacitor ratio in the sensor with an integrated capacitor ratio.

One last advantage that we should emphasize is the control logic—it has been specifically designed to allow easy interaction with a microprocessor. ■

Acknowledgments

The authors wish to thank F. Rudolf for his helpful discussions of micromechanical sensors and M. Schwörer for his help with the logic design. They are also indebted to E. Dijkstra for his general discussions of microprocessor systems.

References

1. J.W. Beyers et al., "A 32-bit VLSI CPU Chip," *IEEE J. Solid-State Circuits,* Vol. SC-16, No. 5, Oct. 1981, pp. 537-542.
2. F. Rudolf, "A Micromechanical Capacitive Accelerometer with a Two-Point Inertial-Mass Suspension," *Sensors and Actuators,* Vol. 4, 1983, pp. 191-198.
3. C.D. Fung and W.H. Ko, "Miniature Capacitive Pressure Transducer," *Sensors and Actuators,* Vol. 2, 1982, pp. 321-326.
4. W.H. Ko et al., "Multiple ISFET with Integrated Circuits," *Proc. Int'l Meeting on Chemical Sensors* (T. Seiyama et al., eds.), Elsevier Science Pub. Co., Amsterdam and New York, 1983, pp. 496-500.
5. M.G. Degrauwe et al., "Adaptive Biasing CMOS Amplifiers," *IEEE J. Solid-State Circuits,* Vol. SC-17, No. 3, June 1982, pp. 522-528.
6. K.R. Stafford, P.R. Gray, and R.A. Blanchard, "A Complete Monolithic Sample/Hold Amplifier Using Compatible Bipolar and Silicon-Gate FET Devices," *IEEE J. Solid-State Circuits,* Vol. SC-9, No. 6, Dec. 1974, pp. 381-387.
7. R. Poujois and J. Borel, "A Low-Drift Fully Integrated MOSFET Operational Amplifier," *IEEE J. Solid-State Circuits,* Vol. SC-13, No. 4, Aug. 1978, pp. 499-503.
8. J. L. McCreary, "Matching Properties and Voltage and Temperature Dependence of MOS Capacitors," *IEEE J. Solid-State Circuits,* Vol. SC-16, No. 6, Dec. 1981, pp. 608-616.
9. E. Vittoz, B. Gerber, and F. Leuenberger, "Silicon-Gate CMOS Frequency Divider for the Electronic Wrist-Watch," *IEEE J. Solid-State Circuits,* Vol. SC-7, No. 2, Apr. 1972, pp. 100-104.

Ernst Habekotté is presently with Sagantec Europa BV, Eindhoven, The Netherlands, where he is involved with analog (bipolar/CMOS) semicustom and full-custom design. He was previously with the Centre Electronique Horloger SA, in Neuchâtel, Switzerland, where he was engaged in the development of intelligent sensors and in low-power analog CMOS design.

Habekotté obtained his PhD in 1982 from the University of Dortmund, West Germany, for his contribution to the development of high-voltage CMOS transistors and circuits. He received his Ir. degree from the Twente University of Technology, Enschede, The Netherlands.

Stefan Cserveny joined the Centre Electronique Horloger S.A., in Neuchâtel, Switzerland, in 1979, where he is presently involved in device modeling and CMOS analog circuit design. Previously he lectured in electronic devices and circuits at the Polytechnical Institute of Bucharest and at the Telecommunications Institute of Oran, Algeria.

Cserveny received the Dipl. Ing. degree in electronics in 1962 from the Polytechnical Institute of Bucharest and the MS degree in electrical engineering in 1973 from the University of California, Berkeley.

Questions about this article can be directed to Habekotté at Sagantec Europa BV, Croy 5A, 5653LC Eindhoven, The Netherlands.

Starting with the first five-volt microprocessor in 1975, Motorola has gone on to produce an entire family of midrange microcomputers and peripherals designed for high-speed operation and maximum efficiency.

The Advancing Technology of Motorola's Microprocessors and Microcomputers

James J. Farrell III
Motorola, Inc.

The appearance and widespread acceptance of the microprocessor in the mid-1970's generated a number of applications for them that had never been implemented. Early microprocessors such as the 6800, Z80, and the 8080 depended on external peripherals to supply them with the necessary RAM, ROM, and I/O devices for communicating and interfacing with other systems. The small size and low cost of the microprocessors and their support peripherals allowed manufacturers to produce equipment that previously could not be produced due to its high cost and/or large space requirements.

One of the earliest uses for the microprocessor was to reduce the size of mainframe computers from a whole room to a desktop. While microprocessors found extremely widespread use in this application, more specialized applications evolved rather quickly. The reason for this was the need to have extremely reliable intelligence that needed only a few discrete components for the control of a given electronic or electromechanical function.

The self-contained package, or microcomputer, would have to contain not only the core CPU, but also all memory. A means of interfacing with the outside world was also required, such as an I/O port and other external functions that would enable the microcomputer to be a stand-alone, self-contained entity in the system. This development first appeared around 1977-1978. Today, microcomputer and microcontroller applications are numbered in the millions, ranging from simple hand-held electronic games to controlling complex electromechanical functions in a space shuttle.

Many systems that utilize microprocessors would not have been designed had it not been for the presence of cost-effective microprocessors. Microcontroller-based systems, while using a microprocessor for their core intelligence, have differing and clearly definable characteristics. The first and most important is low cost. Microcomputer systems as a rule must use high-volume, cost-effective parts—and very few of them. Unlike microprocessor systems, microcomputers usually require only a few thousand bytes of ROM and a few hundred bytes of RAM for use as a scratchpad memory. Typical microprocessor systems usually address from 64K bytes to a few billion bytes of memory. In addition to its core CPU and volatile and nonvolatile RAM, the microcontroller also requires on-chip peripheral functions, some of which are specific to a given application.

0272-1732/84/1000-0055$01.00

1975: the MC6800 microprocessor

The MC6800, which was the first single five-volt microprocessor available on the market, contains control circuitry for the CPU, an arithmetic logic unit that can perform mathematical calculations, two eight-bit accumulators used in number-crunching tasks, a 16-bit index register to access the memory, an eight-bit condition code register that displays the results of previously executed instructions, a 16-bit stack pointer that remembers where stored information was held during an interrupt, and a 16-bit program counter that allows the microprocessor to know where it is in the program. The unit also utilizes instructions in several addressing modes for more efficient performance of its functions.

Processing improvements allowed the MC6800 to run faster than the original design speed of one MHz. The MC68A00 and MC68B00 are the results of these enhancements and allow the processor to run at 1.5 MHz and 2.0 MHz, respectively. At this point the MC6800 architecture diverged into two distinct paths: the MC6808, which contains all the functionality of the MC6800 but added an onboard oscillator; and the MC6809, which did not add any external peripherals to the MC6800 but greatly enhanced the unit's register architecture and software computing power.

1978: the MC6809

The MC6809, while defined as an eight-bit microprocessor because it has an eight-bit external data bus, actually contains six 16-bit internal registers and easily handles 16-bit words internally. The additional registers of the MC6809 were also more useful because additional instructions such as *multiply* were available to the programmer. It also implemented modern software techniques such as position-independent programs that allowed a system manufacturer to use ROM in any available memory space. Modular programs were much easier to use, and high-level languages such as Pascal, Fortran, Ada, and others could be implemented easily in a microprocessor-based system.

1979: the MC68000 microprocessor

Even while the MC6809 was being developed, Motorola was developing a new family of 16-bit microprocessors:

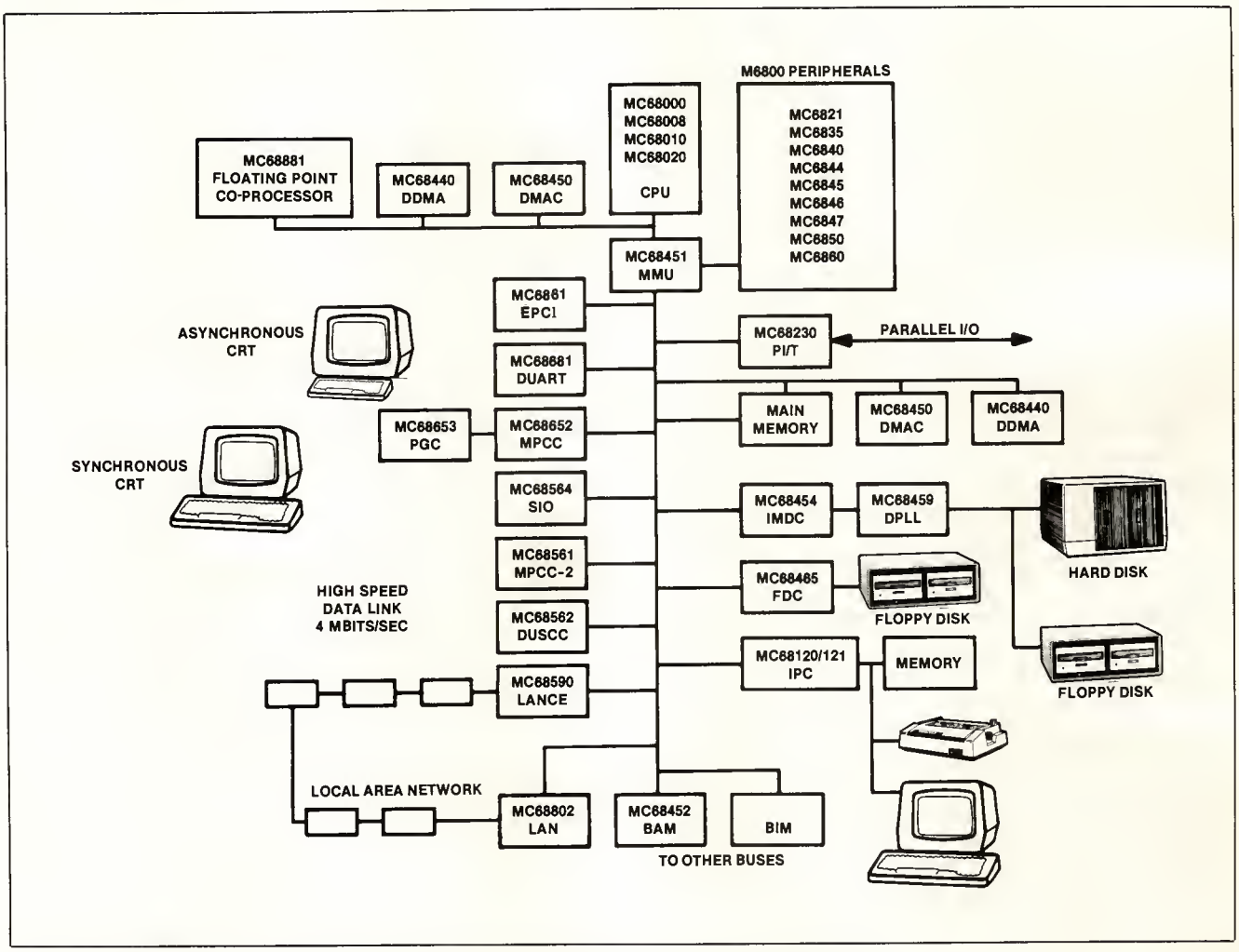


Figure 1. The M68000 family provides a number of peripherals to support the executive CPU.

the M68000 (see Figure 1). The first processor in this family was the MC68000. This unit, while building upon the experience of the MC6809 and MC6800, was a departure from previous designs in that it was intended to be the first general-purpose high-level 16-bit microprocessor. The MC68000 contains 17 32-bit word registers, eight of which are data registers and nine of which are address registers. The two highest-order address registers are reserved for the user's stack pointer and supervisory stack pointer. The eight data registers are not assigned for any specific task, but rather are general purpose. All may be used interchangeably.

The purpose of this architecture was to utilize the MC68000 as an efficient vehicle for all high-level languages, both those in present usage and those that have not yet been developed. The processor supports multiusers and multitasks in operating systems and can easily be built into multiprocessor configurations. The architecture also exploits the advantages of the very dense HMOS technology.

The design goal was to develop the M68000 into a much larger and more complete family of microprocessors and peripherals with total upward compatibility from the earliest microprocessor in the family to the latest. In other words, a code written for the MC68000, which was introduced in 1979, will run on the newest microprocessor of the family, even though the new system may contain new and more powerful instructions. This is because the new instructions occupy areas that were not used in the older processor, while the older instructions are still resident on the new microprocessors in the M68000 family. This provides the system designer with a clean, flexible, general-purpose architecture that can be extended to a variety of future products.

The base MC68000 design has been additionally modified to produce an eight-bit product, the MC68008. This unit contains the entire internal 32-bit architecture of the MC68000 and allows the user to utilize the processor in a much smaller package on an eight-bit data bus. Enhancements to the base MC68000 produced the MC68010, the virtual memory version of the MC68000, which is also identical in internal structure except that this processor allows the efficient design of a virtual memory system. While significant internal enhancements have been made on the MC68010, it can be plugged in directly to an MC68000 socket in an existing system with no additional hardware changes. A new family member, the MC68012, has been added that is essentially an enhanced MC68010. The MC68012 can access two gigabytes (2^{31} bytes) and has a line that indicates a read/modify/write cycle.

Motorola recently introduced the MC68020, a full internal and external 32-bit implementation of the MC68000 that is totally upward object code-compatible with the MC68000 (see Figure 2). It contains all the features and functions of the MC68000 and MC68010, in addition to the ability to accept a coprocessor interface. The MC68020 also has expanded address space, an instruction cache for increased system performance, and an enhanced instruction set for increased flexibility and orthogonality.

The M68000 family of microprocessors allows each unit to be either the executive or peripheral intelligence. The status register of the MC68000 is a 16-bit register divided into two eight-bit bytes. The system byte allows the MC68000 to be the executive of the system, to trace a program to find an anomaly in the code, to present a supervisory bit that determines the status of the processor, and to contain a three-bit interrupt mask that allows eight levels of interrupt.

The user byte uses five bits as a condition code to display to a program the results of a previous instruction execution. Unlike Motorola's eight-bit microprocessors, the MC68000 family uses an asynchronous bus, which means easy interfacing of either very slow or very fast peripheral devices. However, should standard M6800 peripheral devices be used with an MC68000, the latter also has the capability to operate with a synchronous bus. The MC68000 is presently offered in frequencies of up to 12½ MHz, and higher frequencies will be available in the future. Some types are able to operate at temperatures of up to 125° C and as low as −55° C.

1979: the early microcomputers

The MC6802 was the first of the MC6800 microprocessors to move toward becoming a microcomputer. It contains 128 bytes of on-board RAM and its own on-board oscillator, allowing the system designer to significantly reduce the parts count in his or her circuit design. The RAM also allows 32 bytes to be retained in a standby mode at very low power when the microprocessor is not in operation or in case the ac power line fails. The MC6802 has an internal software architecture that is identical to the MC6800.

The MC6801 evolved from the MC6802 and remains one of Motorola's highest-level microcomputers. The MC6801, in addition to the 128 bytes of RAM found in the MC6802 and an on-board oscillator, also has the ability to utilize a 2K-byte internal ROM, or to use external memory as required by the system. An enhancement to this part, designated the MC68701, has replaced the 2K-byte ROM with a programmable ROM called an EPROM. These 2K

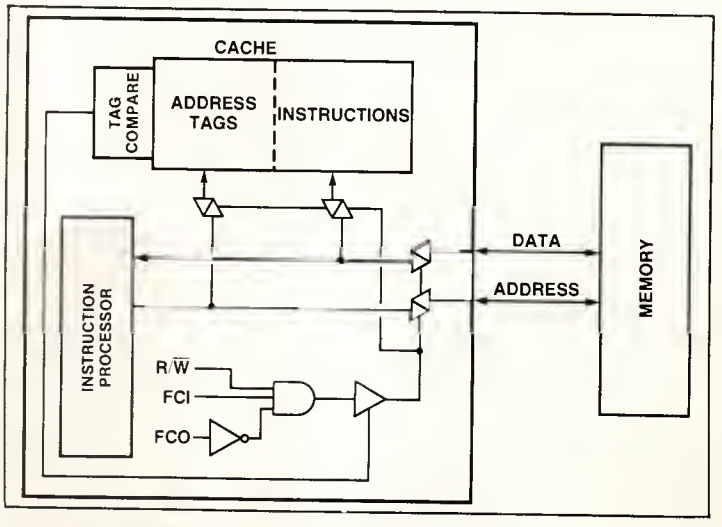


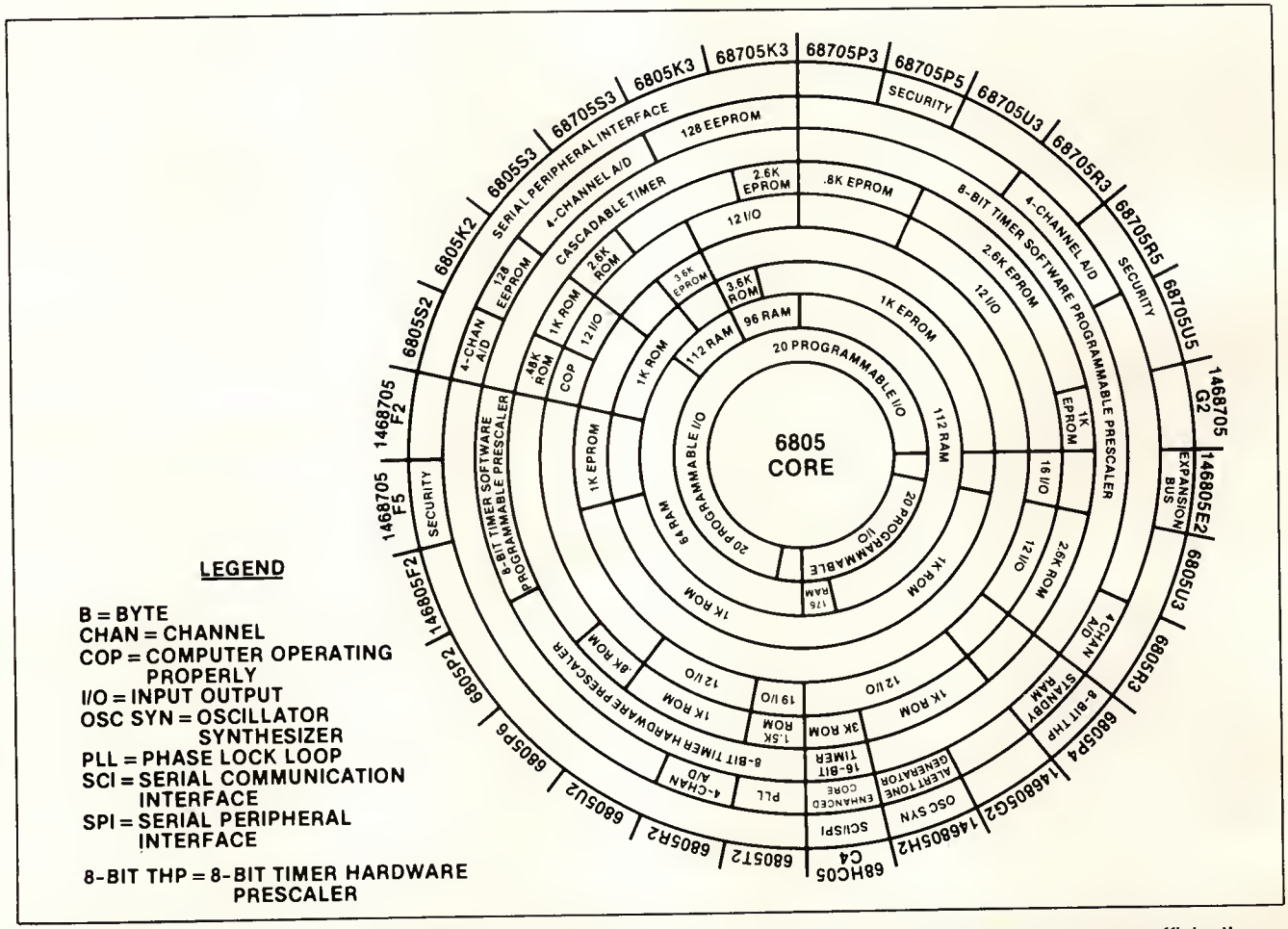
Figure 2. The MC68020 contains an instruction cache to execute code quickly and efficiently.

bytes of EPROM are programmed electrically and can be erased by exposing a window in the package of the part to ultraviolet light. A ROM-less version of the MC6801 is also available. This version, called the MC6803, supplies RAM, an expansion bus, and the other internal features on the MC6801. The MC6801 has a complete MC6800 instruction set plus additional instructions such as multiply, an internal clock generator with a divide-by-four output, a serial communications interface, and a 16-bit multifunction programmable timer. An enhanced version of the MC6801 is available, designated the MC6801U4, which has increased the ROM size to 4K bytes and the RAM size to 192 bytes. The MC6801U4 also has an enhanced timer.

1981: the M6805 microcomputer family

The success of the MC6801 brought attention to the need for a midrange family of microcomputers that could specifically address certain microcontroller tasks requiring less generic functionality, a lower price, and a wider variety of types than the MC6801 offered (see Figure 3). Motorola's M6805 evolved as the result of a modular standard building block process in designing a large family of standard microcomputers. In order to be truly application-specific, the microcomputer family has both a CMOS and an HMOS version. First, a modular core CPU had to be available for this family. This CPU contains its own control circuitry and arithmetic logic unit. The instruction set is identical among all HMOS and CMOS types. The HMOS and CMOS CPUs only vary in that the CMOS types have two additional instructions, stop and wait, that permit the CMOS microcomputer to go into a semicomatose mode in order to save power. The HMOS type, being dynamic in design, cannot be stopped in this manner and still retain data. Therefore, stop and wait have not been implemented in the HMOS types.

The instruction set used with the M6805 HMOS/M146805 CMOS family is specifically designed for byte-efficient program storage. Byte efficiency permits a maximum amount of program function to be implemented within a finite amount of on-chip ROM. Improved ROM efficiency allows this particular family to be used in applications where other processors might not be able to perform their tasks in the available ROM space. In some cases, a user might wish to include programs for more than one application. The appropriate routine can then be selected by the power-up initialization program. The ability to nest subroutines, in addition to true bit test and bit manipulation instructions, multifunction instructions, and versatile address modes, all contribute to byte efficiency.



LEGEND

B = BYTE
CHAN = CHANNEL
COP = COMPUTER OPERATING PROPERLY
I/O = INPUT OUTPUT
OSC SYN = OSCILLATOR SYNTHESIZER
PLL = PHASE LOCK LOOP
SCI = SERIAL COMMUNICATION INTERFACE
SPI = SERIAL PERIPHERAL INTERFACE

8-BIT THP = 8-BIT TIMER HARDWARE PRESCALER

Figure 3. The M6805 family offers the system designer a wide range of on-board peripheral functions to design systems efficiently.

Once a core CPU had been developed, the support registers were defined. All types contain an eight-bit accumulator or "working" register. They also contain an index register used to "point" to a memory location, a stock pointer for recalling where previous contents of the registers are being held in memory, and finally a program counter that will keep track of programs. In addition to the core CPU and its support registers, each variation of the microcomputer contains a self-check ROM so that most of its vital functions can be tested without using expensive test equipment.

The MC6805 family architecture contains several basic registers. There is a single eight-bit accumulator, a single eight-bit index register that can be used for temporary storage, an 11- to 13-bit program counter, a five- to six-bit stack pointer, and a five-bit condition code register. The M6805 family is available in both HMOS and CMOS implementations. While the on-chip peripherals of the MC6805 family differ functionally, the core processor and memory functions are similar among members, with the exception that the amount of memory varies. The core CPU, CPU control circuitry, arithmetic logic unit, accumulator, index register, conditions code registers, stack pointer, and program counter are identical among all family members. All members also have I/O ports (some may have more than others), as well as timers, counters, prescalers, an oscillator, and on-board RAM and ROM. The ROM in some variations takes the form of EPROM.

The MC6805R2, an HMOS microcomputer, contains a unique four-input multiplexed analog-to-digital converter that allows a full eight-bit resolution to be used by the microcomputer system (see Figure 4). The analog-to-digital conversion system not only selects one of four analog inputs but can also compare its full-scale reference and ground ratiometrically to externally supplied full-scale reference and ground. Other variations of the MC6805 family include a CMOS microprocessor, the MC146805E2, which utilizes external ROM for greater system flexibility in low-power applications. The MC146805F2 is a complete CMOS microcomputer that has the capability of direct LCD drive.

A unique member of the HMOS M6805 family is the MC6805T2, which, in addition to all of the 6805's standard features, has a phase lock loop capability. The internal circuitry contains a variable divider, a reference divider, and phase capacitor that generates a correction voltage for any detected deviation between the input frequency and the microcomputer-generated internal frequency. Both the HMOS and CMOS variations of the M6805 family have members with on-board EPROM to permit software development before high-volume ROM-based parts are ordered, or for use directly in production.

1984: the MC68HC11 microcomputer

Motorola recently announced a new type of microcomputer, designated the MC68HC11 (see Figure 5). This new model relieves the programmer of many time-consuming and repetitive software chores and will support many

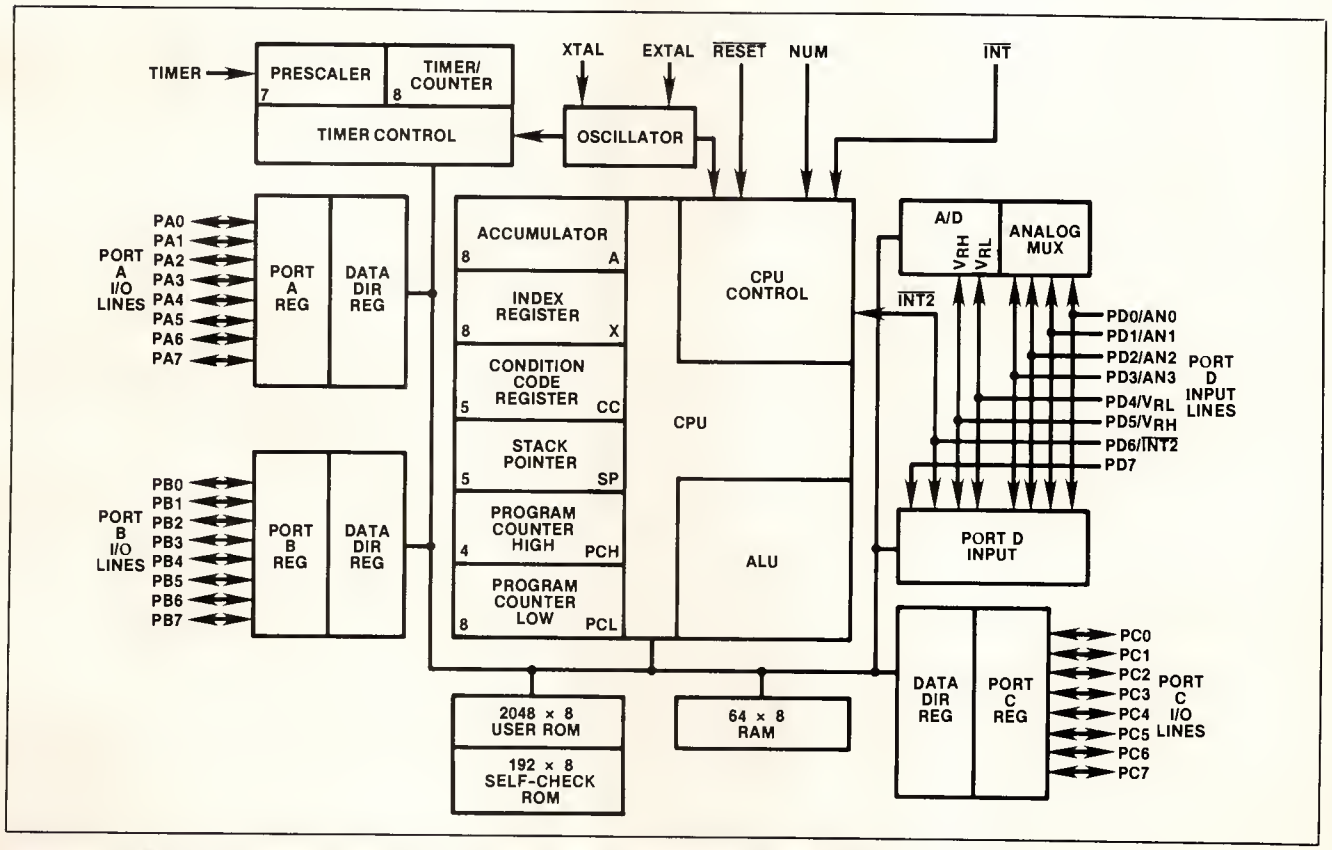


Figure 4. The MC6805R2 provides an analog-to-digital converter as well as several other functions.

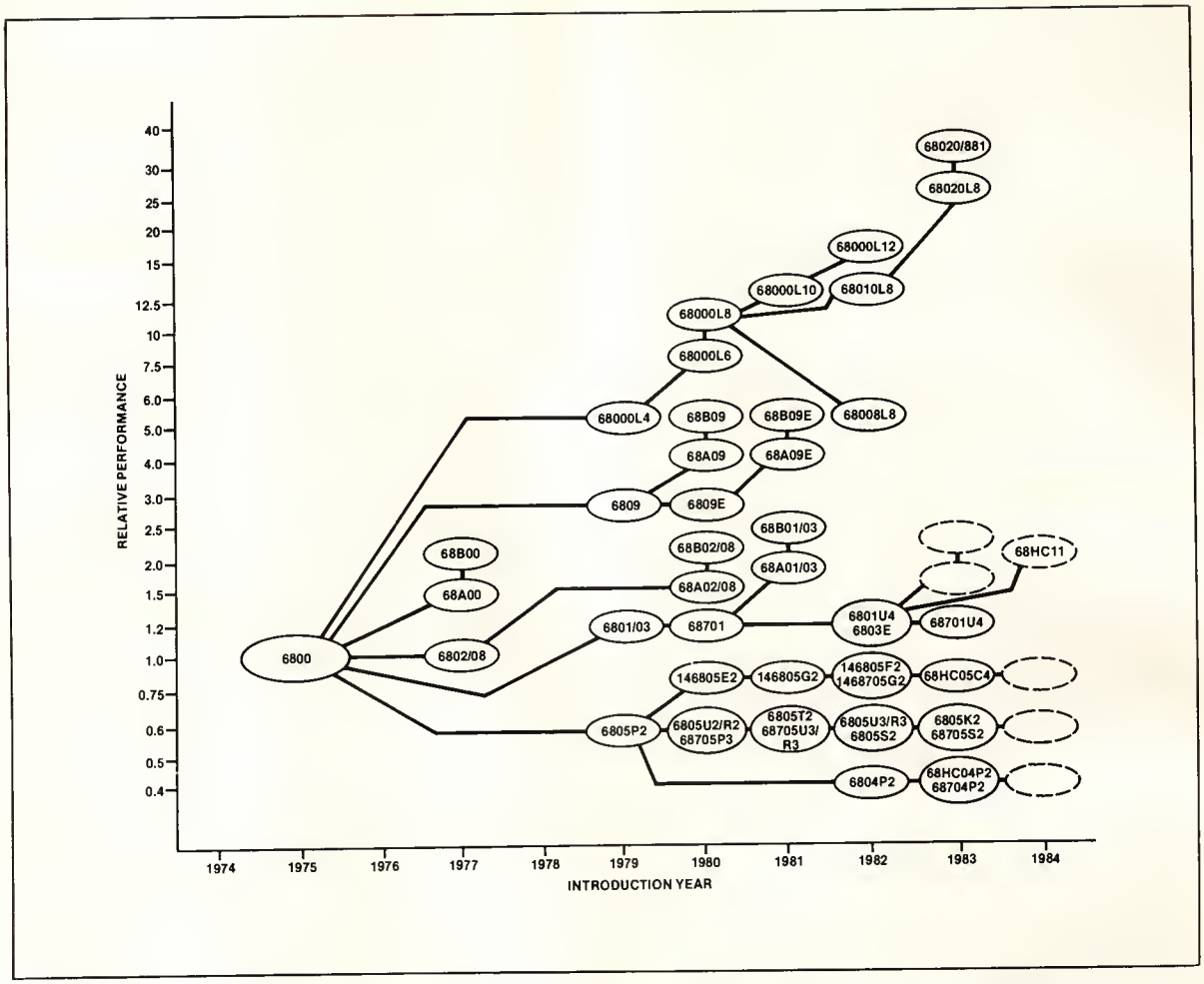


Figure 5. The current M68000, M6804, M6805, and M68HC11 families have all evolved from the M6800 family.

users. It has been designed using the latest HC-type CMOS technology, which allows for high-speed operation while dissipating extremely low power. Lower power dissipation has the double effect of increasing both the microcomputer's reliability and the system power supply's reliability by requiring less output current. This effect is most pronounced in smaller systems.

The nonvolatile memory portion of this microcomputer contains 4K bytes of ROM (or HCMOS EEPROM, depending on which variation is used) plus an additional 512 bytes of HCMOS EEPROM. For scratchpad memory, the unit also has 256 bytes of RAM that is retained in standby mode, using very little power. The architecture of the microcomputer, which is based on the popular MC6801, contains the entire instruction set of the 6801 in addition to several enhancements, such as an additional Y index register. The second index register allows block moves to be implemented very easily. This is a major software enhancement that permits the programmer to save several lines of code when a table has to be moved from one area of memory to another. An enhanced 16-bit timer contains three input capture registers, five output compare registers, a prescaler, and an improved interrupt capability. Three additional features—a computer-operating-properly watchdog timer, a real-time interrupt, and a pulse accumulator feature—permit virtually all of the timing needs of most systems to be accomplished with a minimum of software and without additional parts. In addition to its parallel I/O ports, the unit contains two independent serial I/O subsystems, as well as a 16-channel multiplexed analog-to-digital converter (eight external, eight internal) that utilizes the successive approximation technique of deriving an eight-bit result.

The MC68HC11 subsystem, integrated with the enhancements offered in software, hardware, and CMOS processing, offer the system designer an immensely versatile stand-alone system. The instruction set contains all the instructions of the MC6801 plus a number of additional instructions for a total of 91. Two instructions will accomplish a divide (two forms) and a compare (five forms) for the D accumulator. Bit manipulation instructions such as setting and clearing bits within a given byte, and the ability to branch on a given bit being set or clear, are also available. These bit manipulation instructions can operate in three addressing modes to allow the manipulation of any location in the 64K-byte memory space. Instructions that will operate on the new Y index register, paging instructions, and power-saving instructions such as stop and wait, which had been available on previous microprocessors and microcomputers, are also implemented. The stop and wait instructions allow the microcomputer to go into a semidormant mode while re-

taining all the information in its registers. It will use a very small amount of power in these modes.

The MC68HC11 has the ability to address the full 64K-byte memory map (65,536 locations), from which the memory locations occupied by the 4K-byte ROM may be removed (but remain available for external use) by programming the appropriate EEPROM bits. These bits are in their own separate EEPROM register.

The microcomputer has four modes of operation: the single-chip mode, in which it operates strictly as a microcomputer with the address and data lines unavailable to the outside world; an expanded multiplexed mode, during which it will operate like a microprocessor and be able to access off-board memory; a bootstrap mode for EEPROM programming and self-test for both the chip itself and the end user's system; and an expanded test mode for factory testing purposes. A powerful bootstrap ROM is not present in the memory map while the MC68HC11 is in a normal operating mode. Modes are selected by dedicated mode select pins.

The MC68HC11 ports are configured in the following manner: port A contains three inputs, five outputs, and the timer I/O; port B contains eight outputs with strobe capability and is also the address port for address lines A8-A15 in the expanded modes; port C contains eight I/O lines and/or latch input ports, which are capable of strobed or handshake operation, or multiplexes the lower eight bits of both the address lines and data lines in the expanded modes; port D has six I/O lines (they may be general-purpose I/O or four for the serial peripheral interfaces and two for the serial communications interfaces), plus a serial I/O; and port E has eight lines that are digital inputs and/or the analog inputs for the analog-to-digital converter multiplexing system.

The 68HC11 timer functions contain a 16-bit multifunction timer similar to the MC6801 but that has been enhanced for greater software versatility. A four-stage prescalar allows division by 1, 4, 8, or 16. It has three input capture registers that have the ability to capture on either the rising or falling edge. It also contains five output compare registers. The serial communication interface subsystem is a full duplex asynchronous non-return-to-zero system. It has a selectable word length of eight or nine bits, eight basic baud rates, and can use additional baud rates by using a prescalar. The independent serial peripheral interface subsystem interfaces easily with low-cost dumb peripherals, such as shift registers, and equally well with intelligent peripherals, such as the MC68HC11 itself, on a master-slave basis. These system features, coupled with the A/D subsystem, provide the user with many efficient software and hardware options at a low resource cost.

Packaging

System and printed circuit board designers have long sought a panacea package that would simply and elegantly solve their layout problems once and for all. The ultimate in simplicity for an integrated circuit package is supposed to resolve all degrees of VLSI complexity into a three-leaded package. One lead would be for power, one for ground, and one for a fiber-optic link. Since this universal package is still only a gleam in some designer's eye, we must examine our options in the interim.

Over the past 15 years, no clear-cut packaging standard has been accepted, though the dual inline package has come close. Presently, well over 90 percent of all integrated circuits shipped are in DIPs, and 90 percent of those are plastic. There are several reasons for this, both mechanical and electrical. The DIP is a stiff-leaded, inherently strong package, available in different materials and with few electrical quirks, that lends itself well to both manual and automatic insertion. Hundreds of companies worldwide have made an enormous investment in equipment to handle DIPs of various pin counts. However, in applications where large numbers of devices must be used on a single board, where the device lead count is very large, or where PCB space is severely restricted, an alternate to the DIP is needed.

Flatpacks, with their 50-mil centered leads, are popular with the military and a small number of other users, but they presently hold a market share of less than one percent. There are indications that even this modest percentage will drop, due in part to the impact of the surface-mounting small outline package. The fact that SO packages are generally limited to 29 pins or fewer precludes their usage in packaging ICs, which require a large number of pinouts. COB, or chip-on-board, packaging has filled a niche in packaging needs for the past five years. Presently used in less than three percent of packaging, mostly in watches and some consumer applications, it is starting to find high appeal for ROMs in the game cartridge market.

The COB package is simply a chip attached directly to a PCB and bonded to pads on the same board (see Figure 6). The chip and the wire bonds are then covered with epoxy or a lid for protection. This type of packaging is acceptable in the consumer market where low cost and small size are important, but the COB has not been implemented in many nonconsumer applications. Nevertheless, the huge expected growth in the consumer market should cause an increase in the COB's market share.

Five years ago, just prior to the introduction of Motorola's MC68000 microprocessor, the decision was made to initially offer this 16/32-bit MPU in a side-brazed ceramic DIP. The MC68000 does not multiplex its address and data lines because it would penalize the system, both in throughput speed and increased system parts count. Due to the separation of the data and address lines, the MC68000 has 64 pins: 16 data pins, 24 address pins (which can directly access 16 megabytes of memory), and 24 pins assigned to power and control functions.

The side-brazed ceramic DIP proved to be an easy implementation of the MPU into the system. It uses standard 0.1-inch PCB design rules and can be readily designed into single-sided PCB applications. However, this DIP is large, requiring nearly three square inches of PCB real estate. In most applications this size is not a problem, but some users need a much smaller package. Further, some users are not concerned with the ceramic DIP's size, but rather its cost. The plastic DIP has an identical footprint to the ceramic DIP and may be interchanged with it without any redesign as long as the ceramic mechanical characteristics are not required by the system's environment. The chip carrier

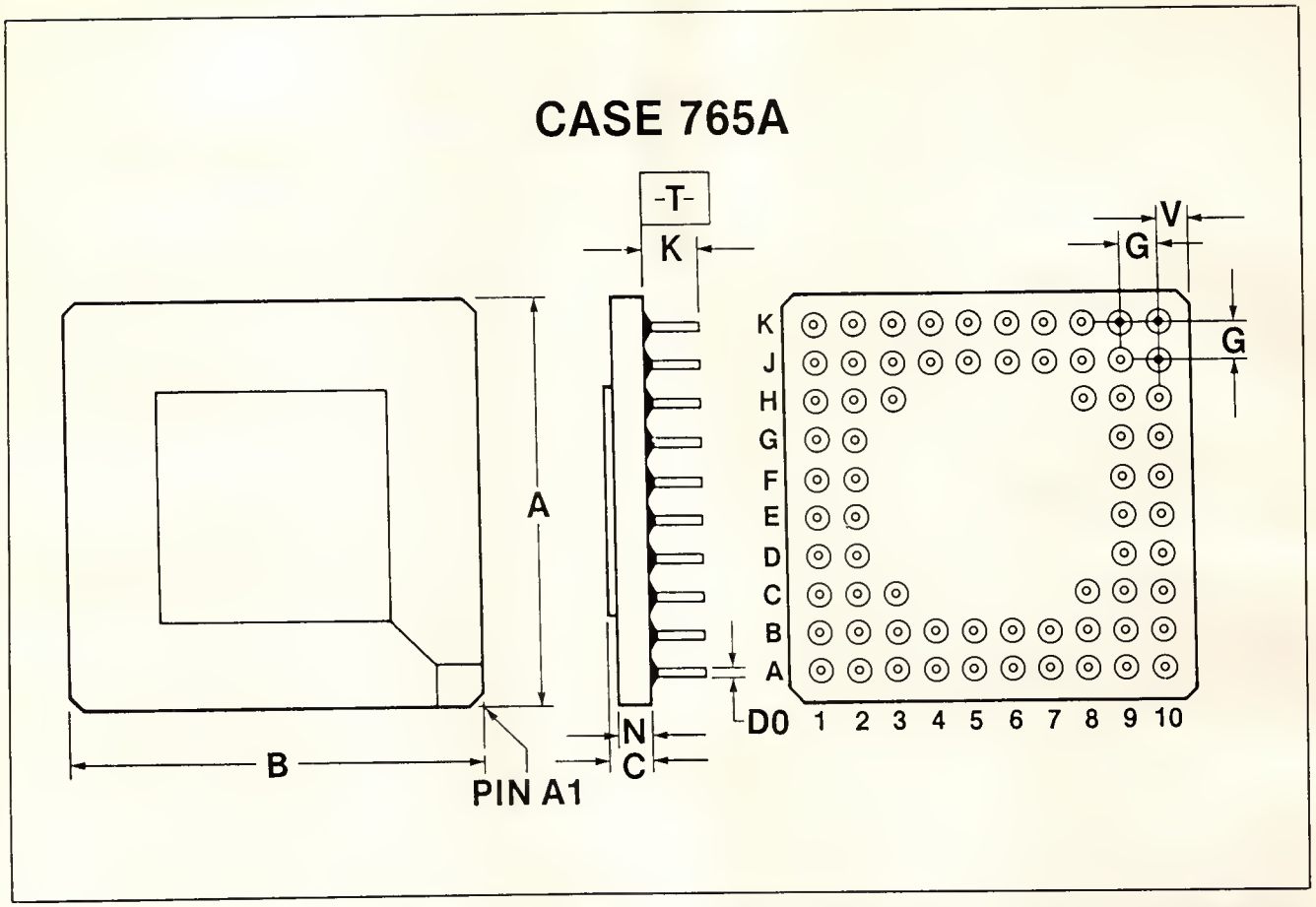


Figure 6. Various packages are used to house integrated circuits. Cost and system environment are usually the prime considerations.

and pin grid array offer very small packages for applications where PCB or substrate space is at a premium.

The Type "C" chip carrier has several desirable features, as shown in Table 1. It can be directly soldered to a substrate, it is an "upright" package, it has a low mounting cost, and it will accept leads to become a leaded (0.05-inch center) plug-in package. In order to implement an effective electrical-short-resistant package, the chip carrier was designed with pads that are only 0.025 of an inch wide. This leaves a 0.025-inch space between metalized areas and reduces the probability of a solder short when mounting the package to an absolute minimum. However, it also presents a problem. The connection pads of the Type "C" carrier are narrow enough to cause alignment problems when it is mounted in a connector (socket). Due to the tight tolerances that would have to be maintained on both chip carrier and connector, no major manufacturer has committed to the production of a connector for the Type "C" chip carrier. By contrast, the Type "A" chip carrier had several manufacturers producing connectors for it. The contact pads on the Type "A" chip carrier measure 0.036 of an inch, which eliminates the connector and causes the pin numbering to be backwards compared with the Type "C" carrier.

The solution was the introduction of a new chip carrier called the Type "B". This chip carrier is identical to the Type "A" mechanically, except that it mounts upright in the Type"A" connector and its pin numbering is identical to that of the Type "C," thereby avoiding PCB layout confusion. The Type "B" chip carrier can be mounted in the Type "A" connector.

The package decision by most users will probably be reduced to available PCB space versus cost. In the least space-restricted applications operating in a normal, non-hostile commercial environment, the plastic DIP (MC-68000GXX) would be the preferred package—first because it has potentially the lowest mounting cost, and second because it is the lowest priced package. It can be socketed or soldered directly into the PCB. Since it uses standard 0.1-inch pin spacing, it will conform easily to current board layout rules—single-sided, double-sided, or multilayer.

The criteria and characteristics of the side-brazed ceramic package are similar to those of the plastic, except the ceramic package will be used where a harsher environment is present, burn-in is required, or military qualification testing must be performed. The ceramic side-brazed package is the most expensive one, but it was the only package initially offered for the MC68000. Now that the plastic version is available, many customers will probably change over to it. Of course, this will require no system modifications.

The Type "B" and Type "C" chip carriers can solve the space problems that many system manufacturers encounter, since they require only about one-third the space required by a DIP and can be purchased with or without

Table 1.

The primary mechanical and cost considerations among packages.

FEATURES	JEDEC LEADLESS CHIP CARRIERS A	B①	C①	DIP CERAMIC	DIP PLASTIC	QUAD SURFACE MOUNT PLASTIC	PIN GRID ARRAY CERAMIC
SOCKETS/CONNECTORS AVAILABLE	YES	YES	NO	YES	YES	YES	YES
DIRECT SOLDER ON	NO	NO	YES②	YES	YES	YES	YES
PIN/TERMINAL COUNT MIN/MAX	14/156	14/156	14/156	6/64	6/64	16/156	40/225
PIN SPACING (MILS)	50	50	50	100	100	50	100
LEAD RESISTANCE (R MAX. IN OHMS)	0.2	0.25	0.5	0.2	0.1	0.1	0.25
LEAD CAPACITANCE③ (C MAX. IN pF)	2	2	2	7	4	2	2
PACKAGE COST④⑦	3	4 ⑤	5 ⑤	2	7	6	1
REQUIRES CONNECTOR/SOCKET	YES	YES	NO	NO	NO	NO	NO
MINIMUM MOUNTING COST④⑦	1	2	5	4	7	6	3
MINIMUM PC BOARD AREA⑥(IN2)⑦	1.25-1.35	1.25-1.35	1.0	2.9	2.9	1.0	1.0
MAXIMUM HEIGHT WHEN MOUNTED⑥(IN)⑦	0.28-0.45	0.28-0.45	0.12	STD	STD	0.15	0.2

* ALL CHIP CARRIERS ARE JEDEC STANDARD LEADLESS TYPES.
① BOTH B AND C HAVE THE SAME FOOTPRINT AND TERMINAL NUMBERING.
② ON ALUMINA SUBSTRATE.
③ THE LEAD CAPACITANCE VARIES LITTLE BETWEEN THE A, B, AND C LCC PACKAGES.
④ THIS RATING IS RELATIVE WITH 1 BEING THE MOST EXPENSIVE AND 7 BEING THE LEAST EXPENSIVE.
⑤ EQUAL COSTS.
⑥ THIS IS THE RANGE OF CONNECTOR SIZES, THAT WE KNOW OF, THAT ARE AVAILABLE.
⑦ FOR THESE EXAMPLES A MC68000 (64 I/O) WAS USED.

the stringent testing of military requirements or burn-in. In very tight applications the Type "C" may be soldered directly to an alumina substrate and maintains a profile height of less than one-eighth of an inch.

Mechanically, 64 pins is felt to be the maximum pin count for the DIP. These packages will continue to be produced indefinitely for the MC68000, MC68010, MC68008, and peripherals, but future high pin count (greater than 64) products, as well as current products, will eventually be offered in a pin grid array. The PGA has been accurately called a "chip carrier with pins." The 10×10 PGA on 0.1-inch centers offers the user a one-square-inch solution to PCB real estate shortage problems but complicates matters with a multilayer board. Somewhat larger PGAs using 0.1-inch pin centers but only two rows of pins around all four sides overcome this problem at the expense of board space, but it appears to be a desirable compromise.

The dramatic drop in prices of eight-bit microprocessors and microcomputers during the past five years has generated the need for yet another package type—the plastic quad surface mount. The QSM solves many problems of current packaging. First, it is very cost-effective. While chip costs and prices have declined, the cost of packages has not. As a result, packaging represents a significant percentage of the cost of many IC products. Second, it is small, which suits many applications that involve severe space restrictions. Third, its 0.05-inch centered leads can be increased in number without developing serious mechanical or electrical problems. Finally, its compliant (movable) leads allow it to be socketed (connected by connector) or soldered directly onto the surface of thermally dissimilar material such as the fiberglass of a PCB. The soon-to-be-introduced super-eight-bit microcomputer, the MC68HC11, will be offered in a 52-lead QSM. ■

James J. Farrell III is the manager of technical communications for Motorola's MOS Integrated Circuits Group. Before coming to Motorola, he spent 10 years with Electronic Associates, Inc., working in analog/hybrid computer development. Earlier, he worked on hybrid ICs and power transistor applications for Bendix Semiconductor.

Farrell graduated from the US Armed Forces Institute in Tokyo and is a member of the *IEEE Micro* Editorial Board. He has published widely in the US and abroad.

Questions about this article can be directed to the author at Motorola, Inc., 3501 Ed Bluestein Blvd., Austin, Texas 78721.

microREVIEW

by David L. Hannum
AT&T Information Systems
Room 59-3A37
99 Jefferson Road
Parsippany, NJ 07054

The Fujitsu 16s comes in three boxes—the mainframe, or base unit, the keyboard, and the monitor. Fujitsu, or rather their PR firm, provided me with a dual-floppy version rather than the newer Model 16sx, which has a hard disk. However, there are few important differences. Unboxing and connecting the system together was a breeze, and the user manual does an excellent job of getting one started. Even without it, the markings are good enough to enable one to couple the system and ready it for initial turn-on.

One immediately notices that the base unit is somewhat larger than the IBM PC/XT's. It has a larger and therefore less appropriate footprint for the business user. The largeness of the unit can, in part, be attributed to the use of full-height floppy-disk drives rather than the more standard half-height ones.

The Fujitsu 16s comes standard with 128K bytes of RAM, just enough to get started. I requested, and promptly received, a 256K memory expansion card. I only had to unscrew five screws to take the cover off the base unit, and needed to exert only a minimum of effort to insert the new board. However, what I found staring me in the face when I opened the base unit was a 130-pin connector in each expansion slot. This is *not* a standard IBM PC connection, and so one would find oneself limited as to where one could get expansion boards. This connector could also be a problem for some of us less adept with our hands, in aligning the boards and not bending some of those 130 pins. Once I had set the DIP switches, I was ready to insert the memory board. All went well, the first try.

The Fujitsu Model 16s has an informative operator's manual, and it is easy to set up for use. Its MS-DOS and CP/M-86 operating systems provide useful on-line help facilities. However, its lack of IBM PC hardware and software compatibility, and its relatively large footprint, will severely limit its appeal.

The system I received had both CP/M-86 and MS-DOS. Since I lean heavily towards MS-DOS for my personal computer uses, I inserted the MS-DOS disk and powered up the system. The screen lit up in multicolor splendor (my review system came with the color monitor), displaying for me the amount of memory installed and identifying the peripherals that could be configured. This experience also showed me that the resolution was no better than that on the IBM PC and PC/XT monitors and systems.

The things one notices as one goes about working on the Fujitsu 16s are the fan noise and cycling, as well as the noise made by the disk drive door latches and by the drive heads. However, the noise is in contrast to the quietness of the drive once the disk has been inserted and the drive door is closed.

MS-DOS is a pleasant surprise on the 16s. The standard set of commands are included, plus an excellent, on-line help facility which gives a synopsis of each command as well as its basic syntax. I must note that if you are accustomed to an IBM-PC-type keyboard, you will have to retrain to be proficient on this one. Also, the keyboard's key click is irritating, though this feature can be squelched with a single command.

I received my unit with the operating systems previously mentioned, Supercalc

3, and Wordstar. (It should be noted that no software is bundled with the 16s.) I loaded Wordstar first; the documentation was well done and complete. However, the disk was empty—blank, no Wordstar.

Since I had loaded MS-DOS, I decided to perform an experiment. As I have stated, or at least indicated, the Fujitsu 16s hardware is not IBM-PC-compatible. But is their operating system? They have indicated in their advertising that it is. I attempted to load my own IBM-PC-compatible versions of Visicalc, Multiplan, TK!Solver, and Wordvision in several different ways, none of which worked. On my scorecard, the 16s gets a zero for IBM PC software compatibility.

The Fujitsu version of Supercalc 3 was easy to use. It provides the user with an initial menu from which he can enter the program proper. This menu allows the novice to get help *before* he uses the program; it also lets the user select tutorials on the various Supercalc 3 commands.

Next I loaded CP/M-86, which stated that it was compatible with CP/M-80 software. Again, I was pleasantly surprised by its on-line help features and ease of use. However, my contentment stopped there. I had received the Fujitsu version of DR-Graph and was unable to load it and, having no other CP/M software, was forced to cut short my time with CP/M-86. Oh, for quality control!

Living with software incompatibility might not be so bad if Fujitsu had plenty of 16s versions of applications software available—but they do not. Add to this the incompatibility of the hardware and I must consider this machine—for all the quality of its documentation—at least unacceptable according to today's business standards.

Other shortcomings of the Model 16s are its semi-useless A/D port and its equally questionable light-pen port. (It does, however, provide both an RS-232C serial port and a Centronics parallel port, something which even some of the leaders do not supply.) The base unit, as I mentioned previously, is oversized (Fujitsu itself suggests setting it on the floor to free more desk space), and it is not appropriately styled for the American market. The American business executive is looking for sleekness and compatibility, of which the 16s offers neither.

I cannot comment on service and support, since I worked with Fujitsu's PR agency rather than with their customer service department.

My overall rating of the Fujitsu Model 16s, on a 1 to 10 scale, is at most a 4. With some restyling, and with redesign of the hardware and software to ensure IBM PC compatibility, there could be a glimmer of hope for this product.

SYSTEM AT A GLANCE

Fujitsu 16s by Fujitsu Microelectronics, Inc.
3320 Scott Boulevard
Santa Clara, CA 95051
(408) 727-1700

GENERAL

Model	16s
Dimensions	19.25 × 14.375 × 6 inches
Price	16s, $2350 (includes base unit, monochrome monitor, keyboard) 16sx (10M-byte hard disk), $4250 16sx (20M-byte hard disk), $4950

HARDWARE

Processor	Intel 8086
Word size	16 bits
Memory	16s, 128K RAM 16sx, 384K RAM 16s can be expanded to 384K or larger via expansion slots.
Storage	16s, dual 5.25-inch floppy-disk drives 16sx, single 5.25-inch floppy plus a 10M- or 20M-byte hard disk Floppies have 360K bytes of unformatted storage.
Display	13-inch green Optional color monitor, $645
Interfaces	Serial, RS-232C port Parallel, Centronics port A/D converter port Light-pen port
Expansion	5 slots, one dedicated to second processor Slots are *not* IBM-PC-compatible.
Keyboard	PC-compatible, but not identical

SOFTWARE

Operating systems	CP/M-86 MS-DOS Concurrent CP/M-86
Language	Basic (and others)
Word processor	Wordstar (and others)
Spreadsheet	Supercalc 3 (and others)

No software is bundled with the Model 16s. The buyer purchases the packages he needs from among those supported. A limited number of other applications in addition to those shown above are available.

MANUALS

The system comes with an operations guide. Other manuals are provided with the software packages selected.

microLAW

by Richard H. Stern
Law Offices of Richard H. Stern
2101 L Street NW, Suite 800
Washington, DC 20037

Ninth Circuit overturns Data General Decision, rules that software-hardware tie-in is illegal per se

In *Data General Corporation Antitrust Litigation*,[1] a federal trial court (the United States District Court for the Northern District of California) addressed the antitrust consequences of a software-hardware tie-in. The district court found the defendant computer manufacturer's practice innocuous. Its opinion, given the setting, suggested that courts would condone practically any similar software tie-in. The trial court indicated that the dispositive consideration was that the relevant market for computer cases includes a great many products, no one of which enjoys a dominant market share, so that the competitive impact of a computer industry tie-in or similar restriction is necessarily of little consequence. The United States Court of Appeals for the Ninth Circuit has now reversed this judgement in an opinion that suggests that there is little legal room in the United States for any software tie-ins, at least where the software is entitled to intellectual property protection.[2]

Defendant Data General had required its customers to use its RDOS operating system software only on its Nova CPUs. Plaintiffs Fairchild and Digidyne unsuccessfully sought to market Nova-emulator CPUs, and sued Data General for allegedly foreclosing them from the market. They argued that a significant number of their potential customers (OEMs) could not buy CPUs from them because the OEMs were "locked in" to RDOS. The applications software that the OEMs owned would run only under RDOS, and the cost of acquiring replacement software that would run under whatever operating system the plaintiffs could supply was so great as to discourage the OEMs from purchasing the plaintiffs' CPUs.

The trial court had held, first, that Data General's requirement that RDOS be used only on Novas was a "tie-in" cognizable under the United States antitrust laws. Second, it had held that the plaintiffs had lost some sales of CPUs that they would have made to OEMs but for the tie-in. That left the third and critical question—whether Data General had sufficient economic power in the relevant market to impose an appreciable restraint on competition. The jury verdict, after 45 days of trial, was for the plaintiffs. But the trial court granted the defendant's motions for a judgment notwithstanding the verdict and for a new trial.

The court's opinion suggests that there is little legal room in the United States for software tie-ins, at least where the software is entitled to intellectual property protection.

The trial court ruled that no reasonable jury could have found, from the evidence before it, that Data General had sufficient economic power, because of its ownership of RDOS, to restrain CPU trade appreciably. The main points in the trial court's opinion were:

- The proper setting in which to gauge Data General's and RDOS' economic power is the spectrum of products against which Novas and the plaintiffs' products, 16-bit CPUs, compete in the marketplace. The relevant tied-product market is all minicomputers and all microcomputers, combined. By the same token, the relevant tying-product (software) market is all operating system software for all such computers, regardless of whether the software is fully compatible with computer programs written to run under RDOS.
- In that relevant market, the Nova faced strong competition from other computer manufacturers and had only a relatively small market share. Also, many operating systems existed—perhaps over 100—that could run on a minicomputer or microcomputer.
- The plaintiffs' argument that they could not sell to OEMs "locked in" to RDOS, because the applications software those OEMs own runs only under RDOS and would be costly to replace, was of no effect. The "lock-in" could not have happened. If it did happen, it was of no moment. The locked-in OEMs account for only a small share of the total market. Moreover, the plaintiffs could have and should have written their own operating system software rather than expect a "free ride" on Data General's.

On appeal, the Ninth Circuit restored the jury verdict, ruling that the facts of the case "abundantly" satisfied the legal requirements for finding an illegal tie-in.

RDOS gave Data General enough economic power to restrain trade appreciably in the sale of CPUs. In sustaining the jury verdict, the Ninth Circuit disapproved the district court's allowing a 45-day trial over what was the relevant market, an issue that the trial court had characterized as the "critical issue" in the case. In the court of appeals' view, it was not necessary to show that Data General had economic "power over the whole market for the tying product" (RDOS), although of course that would more than prove the plaintiffs' case. All that was necessary to make the RDOS-Nova tie-in illegal per se under the United States antitrust laws was proof that "an appreciable number of buyers" yielded to Data General's tie-in demand because of their preference for RDOS, and that if not so "forced" they would have preferred not to buy Novas. It did not matter that another appreciable number of buyers felt otherwise. Thus, to ascertain the material facts, no elaborate economic analysis of the relevant market was needed.

The Ninth Circuit concluded that the jury had had before it "abundant evidence that Data General's RDOS was distinctive and particularly desirable to a substantial number of buyers, and could not readily be produced by other sellers." First, RDOS was considered "the best [software] in the industry, the most comprehensive, compatible, field proven, and rapid" operating system. Experts, customers, and even competitors so testified; further, Data General itself had made such statements in promoting the sale of RDOS, before the litigation had made its officials more wary or reticent. Second, RDOS was copyrighted. This created a presumption of economic power. The burden of rebutting this presumption of power was on Data General. Moreover, witnesses testified that it was impossible to develop operating system software performing all the functions of RDOS without violating Data General's copyrights and trade secrets, or at least it would cost millions of dollars and years of effort to do so.

The Ninth Circuit also saw "software lock-in" as a true source of economic power. The evidence showed that lock-in had occurred and was a powerful factor forcing OEM customers to use RDOS, which in turn had forced them to buy the tied CPUs from Data General. The court of appeals noted that an unwary Data General manager had written a memorandum stating, "Protection from knock-off products still lies in software licensing restrictions." That comparable (rather than fully compatible) operating system software existed or could be written, a factor the trial court stressed, was immaterial to any already locked-in customer; to use any such software the customer would still have to procure new applications software or at great expense modify his existing inventory of applications software.

The reinstatement of the *Data General* jury verdict is a step away from the new antitrust economics in favor with the present administration toward the older, more conventional antitrust enforcement theories previously in vogue.

One explanation of the diametrically opposite judgments of the appellate and trial courts is that at the time of the trial court's opinion, it was widely doubted that operating system software or other computer programs were protectable by United States copyright law in any meaningful way. Indeed, the trial court suggested that object code was probably unprotectable against competitive replication. Accordingly, there seemed to be little barrier against the plaintiffs' simply patching together their own versions of RDOS and thereby defeating any "lock-in." But in the last several years, the legal tide has definitely turned in the United States—in favor of copyrights for software. The efficacy of such protection was now established, in the Ninth Circuit's view, by the decisions in *Apple Computer, Inc. v. Formula International, Inc.*[3] and *Apple Computer, Inc. v. Franklin Computer Corp.*[4] The Ninth Circuit has thus simply told software proprietors that, since they can protect their software against copying by use of the copyright laws, they must recoup their software development costs, plus whatever profit they need to stay in business, by appropriately pricing their copyrighted computer programs, *not* by tying in hardware, peripherals, or software sales.

The reinstatement of the *Data General* jury verdict is a step away from the new antitrust economics in favor with the present administration toward the older, more conventional antitrust enforcement theories previously in vogue. For software sellers subject to litigation in the Ninth Circuit (the West Coast), which must be practically all of them, the Ninth Circuit's opinion signals considerable risk for software-hardware tie-ins and for forced bundling or software with other software. The freedom in licensing software suggested by the district court opinion is appreciably diminished. To rephrase the unwary Data General manager's memorandum, "Protection from knock-off products *does not* still lie in software licensing restrictions."

References

1. 490 F. Supp. 1089 (N.D. Cal. 1980), 529 F. Supp. 801 (N.D. Cal. 1981). See "Can Software Be Tied to Hardware?" in the February and April 1983 issues of *IEEE Micro* for a discussion of the trial court's opinion.
2. Opinion of June 4, 1984, as yet not officially reported.
3. 725 F.2d 521 (9th Cir. 1984).
4. 714 F.2d 1240 (3d Cir. 1983).

Who should own software?

In this column we have frequently explored the question of software ownership and copyrightability (see, most recently, the April "Microlaw"). We are interested in your views and invite you to make them known via "bingo card" response—please circle the appropriate number on the response card at the back of the magazine:

- I think that the first person to write and market a particular code should own the copyright against subsequent comers, and should be able to stop others' use of the code, even if there is only one way to write a code that meets all of the first code's specifications. **(Circle Number 90.)**
- I think that nobody should own the code when there are only one or a very few ways to write a code that meets all specifications. **(Circle Number 91.)**
- In this situation, I think that the first person to write the code should be paid compensation, but second comers should be allowed to use the code on a royalty basis. **(Circle Number 92.)**
- Other. (Write a letter.)

We will report on the results from time to time.

microNEWS

Testing of 200,000-transistor chip kept manageable

Ware Myers, Contributing Editor

To test Motorola's first microprocessor, the MC6800, in all possible combinations would have taken two million years, Gary Daniels, vice-president of the Motorola technical staff, said in an invited speech to the International Test Conference in Philadelphia last October. "That is the essence of the problem of testing microprocessors," Daniels pointed out. "It isn't that we are not willing to do it, it's just that you are not willing to wait that long."

The first test circuits built into a Motorola microprocessor were in the MC6802 in 1977. This device, basically a MC6800 plus a RAM and a clock, had 11,000 transistors. In contrast, Motorola's latest microprocessor, the 32-bit MC68020, contains 200,000 transistors. This increase in size has greatly multiplied the testing problem.

The testing of commercial VLSI is hemmed in by a number of constraints. The development time to generate the test patterns must not be too long; the time to run the test patterns mut be only a few minutes; circuits added to the chip to enhance testability must occupy a limited area so as not to reduce yield unduly; test coverage must be high so that users may be assured of good parts. These constraints all finally reduce to a matter of cost, and minimizing cost is the result of an appropriate balance among these constraints.

In a paper presented to this same conference, Motorola's John Kuban and John Salick showed that a "judicious mixture" of functional testing and structured testing "makes the MC68020 a highly testable chip without significantly affecting die size." By itself, functional testing of VLSI devices may require a prohibitive amount of engineering time and/or produce poor fault coverage, they claimed. Similarly, fully structured testing can grow the die size enough to impact yield. Test planning was aimed at three goals: to keep test development time limited to a reasonable percentage of chip design time, to reduce the expense of simulation, and to ease the test grading burden by providing known fault coverage over a good portion of the chip.

Designing to make a chip more easily testable is often divided into three categories, T. W. Williams of the IBM General Technology Division, Boulder, Colorado, explained in his plenary lecture at the International Conference on Computer Design at Rye, New York, the previous week. The three are ad hoc design, structured design, and built-in self-test. Ad hoc design involves partitioning a large design into smaller pieces for separate testing; it may take advantage of the natural bus structure of the design in effecting this partition. Structured design adds logic to the basic design, such as in the level-sensitive scan design that IBM developed. In built-in self-test, some of the test circuitry is built into the chip itself.

Kuban and Salick made use primarily of the first approach. They used the bus structure of the MC68020 to separate the ROMs, cache memory, execution unit, and some of the PLAs. However, the existing buses were not sufficient to segregate some of the other PLAs, so they provided a signature register and multiplexers to complete the partitioning. Only one built-in self-test, providing test microcode to a PLA, was employed.

The logic added for test purposes—16-bit signature register, multiplexers for the ROMs and PLAs routing and "test only" logic—added less than three percent to the area of the MC68020.

Design is often a matter of trade-offs. The design of their ad hoc test logic took more time than a scan technique might have, they admitted. On the other hand, use of a scan design would have increased die size more than the method they used. Still, the existing bus structure made it "relatively easy to create test partitioning for the embedded structures." On balance, they feel that the higher yield they expect offsets this extra design time.

Test time will be acceptable, the authors reported, although actual production test time had not been established at the time of writing. "The savings in text-generation costs and the known fault coverage more than outweigh the increased test time," they added.

"The size and complexity of this microprocessor promised to create a test nightmare," Kuban and Salick said in conclusion, "but we were able to keep the problem manageable. Buses, test microcode, and the signature register partitioned one large problem into several smaller ones. Partitioning and high-level simulation reduced computer costs. Algorithmic test generation automatically produced known fault coverage for selected modules."

First meeting of working group on open systems architecture announced

With the advent of standards in the area of operating systems, the industry is reaching a level of maturity at which a model for system-level standards is appropriate. Such a model would span bus-level standards (P896 Futurebus, P1014 VME Bus, Multibus II, Nubus, etc.), operating-system-level standards (P855 MOSI and P1013 Unix), and local-area network standards (P802 and the ISO efforts). A working group to consider this concept was approved by the Computer Society Standards Coordinating Committee in October 1984. The formation of this group is a response not only to the interest in a standard architectural model but also to the concerns raised recently by Gordon Bell in the June issue of *Computer* and by Maris Graube, chairman of P802, at the recent NBS/ISO workhop on the interaction between LAN and operating system standards.

The working group will attempt to define a model, not unlike ISO's OSI—Open Systems Interconnection—model, that permits the clear identification of the interface points between different system levels and provides a common framework for current and future computing standards. Properly structured, this model would encourage the development of elements targeted to specific environments and applications and would permit those elements to be plugged into a well-defined layer of an architecture,

cont'd on page 72

microSTANDARDS

by Robert G. Stewart
Stewart Research Enterprises
1658 Belvoir Drive
Los Altos, CA 94022

Sponsor ballot results

After years of effort, a number of proposed micro-related standards have now been essentially completed by the working groups and are ready for "sponsor ballot" or are already being balloted. The prime problem which exists is the requirement of the IEEE Standards Board that 75 percent of all ballots must be returned, and that 75 percent of the returned ballots must then approve the draft, for the proposed draft to pass. The difficulty is getting 75 percent of the sponsor body, which is a subset of the Technical Committee on Microprocessors and Microcomputers, to return the ballots in the first place. Very few changes are typically made in the drafts from the working groups. Usually the vote is heavily in favor of adoption, with occasional changes requested.

The status of several standards is shown in the table below.

Status of standards.

PROJECT	SUBJECT	STATUS
694	Assembly Language	Passed, 92 percent
695	MUFOM—Relocatable Object Code	Passed
754	Floating-Point Arithmetic	Passed
755	HLL for Microprocessors	Insufficient returns yet
854	Radix-Independent Floating-Point	Public comment phase
855	MOSI—Micro Op. Sys. Interface	Passed as trial-use standard
949	Media-Independent Info. Transfer	Passed, 78 percent, checksums added

Are more 32-bit bus standards needed?

Three 32-bit buses are already being standardized by working groups of the Microprocessor Standards Committee: P896—Futurebus, P970—Versabus, and P1014—VME Bus. At the P896 meeting held at Wilsonville, Oregon, in April 1983, a once-in-a-lifetime opportunity was missed when Intel Corporation declined to cooperate with TI and the P896 committee in jointly creating a high-performance 32-bit bus. P896 had settled on an asynchronous protocol somewhat similar to that of the DOE's Fastbus. TI, with guidance from MIT, had taken some parts of P896 but had chosen a synchronous, clocked protocol. Intel decided to also use a synchronous protocol, but insisted on their own design. Paul Borrill, P896 chairman, was able to alert Andy Grove to inadequacies of Intel's initial conceptions, which had the boards

based on the IEEE 796 (Multibus) form factor. Intel moved to the Eurocard form factor and adopted a form of P896's arbitration method, but otherwise followed their own course.

The Microprocessor Standards Committee voted in August to ask for Project Authorizations Requests so that both TI's and Intel's version of a synchronous 32-bit bus can be developed as separate IEEE standards. I, for one, believe this is a gross misuse of the IEEE Computer Society and the IEEE. The companies' gain clearly involves marketing—they can advertise their own designers' bus as an IEEE standard. The IEEE working group which has cognizance in the area, P896, was not provided copies of Intel's bus specification until months after it was released to the public. Hubert Kirrmann has written and circulated in the P896 mailing a detailed comparison of the three buses and pointed out their advantages and shortcomings. Gordon Bell has suggested the need for bus birth control in his article on standards in the June 1984 *Computer*. I agree. It is not appropriate for marketing groups in companies to determine the nature of IEEE standards. In Intel's case, they dominated the technical individuals on their design staffs and precluded them from even participating in the activities of the existing IEEE committee. Incompatible cards having the same form factor and different pinouts and plugging into the same DIN sockets can only lead to unnecessary problems in the years ahead—like burning out when they are inserted.

Benchmark working group reactivated

Steve Diamond has revitalized the P856 Microprocessor Software Benchmark Working Group and is soliciting participation from those interested in standardization of tools for microprocessor performance measurement. If you are interested, contact

Stephen L. Diamond
National Semiconductor
MS D3668
2900 Semiconductor Drive
Santa Clara, CA 95051
(408) 721-4817

A scale for rating microcomputers

Never having been one to shirk from trampling in swampland, I'd like to share with you my scale for assessing the merit of a microcomputer. The scale deals with the hardware, software, and manufacturer-related aspects of the micro. Add up or subtract all the appropriate points. The total is the scale value for the system. The slash means "per." If you'd like to try it out on your system, you can let me know the results in the "Comments" section of the bingo card at the back of the magazine.

ATTRIBUTE	SCALE POINTS
HARDWARE	
1. Microprocessor	
a) Clock frequency	+1/megahertz
b) Word width	+2/byte
c) Nonsegmented addressing	+6
d) Cache	+3
e) Uses IEEE P694 mnemonics	+2
2. Bus	
a) Motherboard-daughterboards	+4, then +1 for every 3 daughterboards
b) IEEE standard	+4
c) DMA	+2
d) Data width	+2/byte
e) Throughput	+1/megabyte/second
3. Memory	
a) Size	+1/64kB to 1MB, then +1/MB above that
b) Access time	−1/50 nanoseconds
c) Static	+2
d) Error correcting	+4
4. Front-panel lights and switches (capable of deposit and examine)	+10
5. Printer	+2
a) Letter quality	+4
b) Speed	+1/20 cps
c) Bit-mapped	+3
6. Display	
a) Color	+5
b) Resolution	
High—1024 × 1024 or more	+5
Medium—525 × 525 or more	+2
Low—less than 525 × 525	−5
c) Lines and columns—24 × 80 or higher	+5
d) Bit-mapped	+3
7. Keyboard	
a) Full size	+3
b) Cursor keys	+5
c) Numeric pad (if separate from cursor keys)	−2
d) Bad key location	−5
8. Disk drives	
a) Number	+4/drive
b) Capacity	+2/MB
9. Virtual memory	+5
10. Real-time support	+5

11. Communications	
a) RS-232	+2
b) Modem	+4
c) LAN—IEEE 802	+6
12. EMI suppression	+4
13. Repairability	
a) ROMs or EPROMs (unless programming information supplied)	−5
b) Custom chips	−5
c) Repair time	−2/hr MTTR
14. Reliability	+1/2000 hr MTBF

SOFTWARE	
1. User-friendly	+10
2. Operating system—CP/M, Unix, or MS-DOS	+10
3. High-level languages—Ada, Basic, C, Forth, Fortran, Lisp, Pascal, PL/1	+3 each
4. Assembly language	
a) Assembler	+5
b) Debugger	+3
5. Graphics	+10
6. Automatic I/O interfacing for object code (IEEE P855 MOSI compatible)	+8
7. Relocatable code conforms to P695	+4
8. Floating-point arithmetic conforms to P754 or P854	+4

FEATURES	
1. Weight	−1 for every 2 pounds
2. Size	−1/200 cubic inches
3. Power	−2/100 watts
4. Portable and battery-operated	+5
5. Cost	−4/$1000
6. Style	+4

MANUFACTURER	
1. User-friendly	+5
2. Survivability	+1/each billion dollars in sales (10 max) +1/each 10 years in business
3. Repair locations	+10 if local repair depot
4. Honest advertising	+5
5. Bad advertising	−15
6. Manuals	
a) Software	+1/100 pages
b) User	+2
c) Maintenance	+5

Using this scale, with help from Dave Gustavson, I came up with a scale value of 97 for his IBM PC/XT.

promoting the portability of products from different manufacturers within an end-user environment. Examples might include the ability to change boards (standard bus layer) or processors (standard operating system layer). The model would also encompass memory management concepts (virtual, segmented) and device drivers—the gray areas that lie ill-defined at the boundaries of the existing standards. It was Jim Isaak of Charles River Data Systems who coined the term OSA—Open Systems Architecture—for the effort.

A meeting to discuss the scope, objectives, and schedule for the development of this far-reaching standard-architecture framework will take place at Compcon Spring in San Francisco on Tuesday, February 26, between 9 am and 5 pm in the Cathedral Hill Hotel. The room number will be posted on the Compmail+ (Computer Society electronic mail) bulletin board prior to the meeting and on the notice board at Compcon on Monday, February 25. Architecture-minded experts from every area of computer science and engineering are invited to attend.

The meeting will be chaired by Paul Borrill, secretary of the Computer Society and member of the Governing Board.

Introducing a new editorial board member

Richard Mateosian has been appointed to the *IEEE Micro* editorial board. He is the new product planning manager for National Semiconductor's Series 32000 32-bit microprocessor product line. His principal responsibilities are competitive performance analysis and new product planning. Previously, he held a similar position at Zilog. Before that, he spent more than 10 years as a systems development manager with several turnkey systems firms, and several years as an independent consultant and author. He is the author of many technical papers and two books, *Programming the Z8000* and *Inside Basic Games,* both published by Sybex.

Mateosian received his BS in mathematics from Rensselaer Polytechnic Institute in 1963 and his PhD in mathematics from the University of California at Berkeley in 1969. He is a member of the IEEE Computer Society and of the Association for Computing Machinery, and is active in the IEEE P854 standardization effort for floating-point arithmetic.

Mateosian will assist in *IEEE Micro's* article acquisition and review process.

New board member Richard Mateosian.

X3 announces public review and comment period on proposed Small Computer System Interface

X3, the American National Standard Committee on Information Processing Systems, announces a public review and comment period on draft proposed American National Standard X3.131-198x, the Small Computer System Interface.

This draft proposed standard was developed by X3T9.2, Lower Level Interface, a task group of X3T9, the X3 Technical Committee on I/O Interface. It defines mechanical, electrical, and functional requirements for attaching small computers to each other and to low- to medium-performance intelligent peripherals such as rigid disks, flexible disks, magnetic tape devices, printers, and optical disks. The resulting interface facilitates the interconnection of small computers and intelligent periphrals and thus provides a common interface specification for both systems integrators and suppliers of intelligent peripherals.

The draft is available for public review and comment until April 5, 1985. Copies may be obtained from the X3 Secretariat, CBEMA, 311 First Street NW, Suite 500, Washington, DC 20001. Orders must include a prepayment of $20.00 and a self-addressed mailing label.

X3 announces public review and comment period on proposed Intelligent Peripheral Interface Standard

ANSI X3 announces a public review and comment period on draft proposed American National Standard X3.132-198X, Intelligent Peripheral Interface, Device-Generic Command Set for Magnetic and Optical Disks.

This draft proposed standard was developed by X3T9.3, Device Level Interface, a task group of X3T9, the X3 Technical Committee on I/O Interface. Its purpose is to facilitate the development and utilization of computer systems by providing a common logical interface which permits the interconnection of peripherals with diverse characteristics (disks, tapes, printers, terminals, and so on). The first three sections contain material which is useful across all classes of device that the device-generic command sets can support. The following sections are oriented to particular device classes.

The draft is available for public review and comment until May 4, 1985. Copies may be obtained from the X3 Secretariat, CBEMA, 311 First Street NW, Suite 500, Washington, DC 20001. Orders must include a prepayment of $25.00 and a self-addressed mailing label.

To obtain more information about a product or service featured in New Products, circle the appropriate number on the Reader Service Card at the back of the magazine.

NEW PRODUCTS

New Products Editor: Victor P. Nelson

Panasonic introduces digital optical-memory disk recorder

Panasonic has introduced a DRAW (direct-read-after-write) digital optical-memory disk recorder. The digital OMDR, the first system of its kind, says Panasonic, can be linked up with facsimile lines for transmission or retrieval of digital information and can store 10,000 letter-size documents in an eight-inch-diameter optical disk. The system is an application of Matsushita's optical disk recording technology, which employs semiconductor lasers.

When plugged into a computer, the digital OMDR will store the computer's information. It can also store images from an X-ray machine. The digital OMDR has a large recording capacity—about 1000 times that of an eight-inch, 1M-byte floppy disk or 150 times that of a full-scale computer disk unit.

The recorder's error rate is 10^{-5} (raw) and 10^{-7} (after corrections). It retrieves information in an access time of 0.5 seconds, and its data transfer rate is 5M bytes per second. The fast read/write access is achieved through the use of a single laser diode in the optical head—a very small, fine-focused beam of light driven by a high-powered linear motor. (A future version of the OMDR will also be able to erase.)

The laser drive offers high-speed power response and precise control, Panasonic says. It features a sector precheck, which eliminates a bad sector before recording. The 4/5 modified nonreturn-zero modulation and demodulation gives a high recording density and less DC component.

The digital OMDR, which measures approximately 8 inches (H) × 22 inches (W) × 20 inches (D), has a simple, front-loading format for easy access.

The optical disk is a three-layer structure: a thin-film recording layer of reducing tellurium suboxide is placed on a base material that forms a protective layer on the film. The all-plastic, solid enclosure is resistant to pressure and physical shock, preventing mechanical transformation.

A semiconductor laser beam records information by putting a shading on the disk. For retrieving information, the laser beam just picks up the shading pattern. The recording track scrolls at a 1.65 μm pitch, and the recording area on the disk is divided into 32 radiant sectors. The advancement of digital technology, says Panasonic, makes inputting more precise and retrieving far easier than in analog recording.

The price of the digital OMDR, model TQ 2023, is $34,900.

Reader Service Number 1

Oracle relational DBMS announced for PC/XT and PC/AT

Oracle Corporation has announced the release of Oracle for IBM's PC/XT and PC/AT under the PC DOS operating system. The relational database management system, compatible with IBM's SQL/DS and DB2, is identical to the Oracle that runs on mainframes and minicomputers. Programs written for SQL/DS or DB2 will run unmodified on any version of Oracle, including the PC version.

Oracle also offers networking software that allows PC Oracle to communicate with the IBM mainframe and DEC Vax minicomputer versions of the DBMS. The new facility, called Oracle Link, allows PC users to directly access and update data stored in the shared database on the mainframe or minicomputer, or to copy that data into the database on their PCs and operate independently.

PC Oracle is priced at $1000 per copy with a minimum order of $6000. The software includes the relational DBMS, application generator, report writer, integrated data dictionary, and Oracle Link.

Reader Service Number 2

Design system shortens VLSI development cycle

A VLSI design system based on advanced silicon compilation has been introduced by Silicon Compilers. According to the company, the Genesil Silicon Development System lets system designers as well as integrated-circuit designers describe designs in high-level functional terms and then produce them as VLSI chips with handcrafted quality in only a fraction of the time required to design a custom chip.

For example, says Silcon Compilers, "The Microvax chip we designed for DEC took us five months from the signing of the contract to tapeout. A similar chip designed by conventional techniques might take as long as three years." The Genesil, the company says, is the first system based on silicon compilation methodology.

The Genesil system handles all the VLSI development steps that follow functional description but precede actual chip manufacture. The creative parts of system design are still done by the designer, while all of the time-consuming elements—documentation, layout, timing analysis, and functional simulation—are a cooperative effort of user and machine. However, says Silicon Compilers, the Genesil system does the lion's share of the work.

The system embodies a dual-phase design approach that allows designers to explore design options (the exploratory phase) before engaging in detailed design (the detail phase). In either case, users receive immediate feedback on size and speed that becomes more precise as the level of detail increases. Often, significant design decisions can be made during the exploratory phase that would otherwise have had to wait until actual silicon manufacture.

During the exploratory and detail phases, users can define functional blocks, describe the interconnection relationships, verify logical operations, and analyze critical-path timing. The tooling activity—tapeout and testout—permits the designer to work independently of technology or foundry until ready to commit a design to manufacture. Then, when the designer specifies technology and vendor, the system generates the appropriate tooling.

The Genesil is a turnkey system consisting of a Vax 11/750 superminicomputer with 4M bytes of main memory, a 450M-byte disk storage system, tape storage, and up to four optional high-resolution color terminals. The system software provides such functions as IC definition, functional simulation, timing analysis, place and route, and testout and tapeout.

Silicon Compiler's Genesil Silicon Development System, including hardware and software with NMOS function set, sells for $545,000. A CMOS function set will be available during the first quarter of 1985.

Reader Service Number 3

The Smartline C600 Intelligent Cable from Computer Accessories converts Commodore data and code for use by parallel printers.

Smart cables link Commodores and printers

Two "smart" cables for solving compatibility problems between popular printers and the Commodore 64 and Commodore Vic-20 computers have been announced by Computer Accessories Corporation.

The Smartline C600 and C601 cables solve two problems inherent with connections between the Commodore computers and printers. One is that the Commodore sends serial data, but most popular printers are designed for parallel data input. The other problem is that the Commodore's character codes do not correspond to standard printer codes. The Smartline cables perform both format (serial-to-parallel) and code conversions within the cable, using built-in circuitry embodying special-purpose programs. Program listings, graphics, and other on-screen information can be reliably reproduced in print as they appear on the computer screen.

In addition to its conversion capability, the C601 Intelligent Cable comes with Wordline word-processing software, offering such capabilities as move, delete, and copy (for characters, words, or lines); automatic word wrap; global or selective search and replace; and left and right justify. Wordline is supplied on cassette and comes with a self-adhesive command-prompting strip; users of the Vic 1541 external floppy disk will find it easy, Computer Accessories says, to transfer the program from cassette to disk. Graphline software, also included, lets a Centronics-type printer or a printer supporting the Star Micronics Gemini 10X dot-addressing standard duplicate Commodore on-screen graphics and special characters.

Both Smartline cables work with parallel printers from Anadex, Brother, C. Itoh, Epson, NEC, Okidata, Star Micronics, Transtar, and others.

The Smartline C600 Intelligent Cable is available for $69.95; the C601, with cassette software, is $99.95.

Reader Service Number 4

DMA controller boosts I/O power of iAPX 286, iAPX 86

Intel has introduced an advanced direct-memory-access controller designed to optimize the performance of microcomputer systems using the company's iAPX 286 microprocessor, as well as systems based on the iAPX 86/186 microprocessor family.

The 82258 ADMA controller is aimed at applications that require high-speed I/O processing, high I/O throughput, flexible data communications, and manipulation capabilities. Such applications include data communications systems, multiuser business systems, graphics and engineering workstations, I/O subsystems such as disk drive controllers, and industrial automation systems. According to Intel, ADMA adds I/O coprocessing capabilities to improve overall system performance, especially in data-transfer-intensive environments and disk-based operating systems like Unix.

Intel expects the 82258 to become a standard component in all future iAPX 286 and high-end iAPX 186 system designs. The device was jointly developed by Intel and Siemens Corporation and will be manufactured by both companies.

In operation, the 82258 uses command and data-chaining features to remove I/O processing functions from the central processor. Further performance improvements result from the 82258's 8M-byte-per-second data transfer rate when the controller is used with the iAPX 286's pipelined architecture. This data transfer rate, says Intel, makes the 82258 at least two times faster than any other high-speed DMA controller available.

Input/output management applications can take advantage of the 82258's ability to support up to 35 different data channels. The controller's four-channel design allows high-speed data transfers on all channels. Alternatively, three channels can operate in high-speed mode with the fourth channel initialized as a multiplexer channel supporting up to 32 low- to medium-speed data channels.

Data manipulation is provided through concurrent data comparison, translation, assembly, and disassembly operations. In assembly and disassembly, bytes can be packed into words and words unpacked into bytes to support 8-bit I/O devices in 16-bit systems.

The 82258's on-chip bus interface can be programmed to support both the pipelined iAPX 286 bus and the multiplexed iAPX 86 family bus, with a maximum memory addressability of 16M bytes for iAPX 286 systems.

Intel has begun sampling of the 82258 in 6- and 8-MHz speed selections. Pricing for the 6-MHz version is set at $170 in quantities of 100. Production is targeted for mid-1985.

Reader Service Number 5

Mouse software provides color graphics for IBM PCs

PC Paint is a mouse-based color graphics package for the IBM PC, PC/XT, PC AT, PC jr, and compatibles. Manufactured by Mouse Systems Corporation, PC Paint can be used to create pictures and to enhance standard graphs and charts for text and graphic presentations. According to Mouse Systems, PC Paint is significant because, in addition to providing powerful graphics manipulation capabilities for the IBM personal computer family, it demonstrates the power of the point-and-click user interface.

For creating graphics images, PC Paint features software "painting and drawing tools" such as color bar, line-width box, patterns, shapes, pencil, paintbrush, and spray can. Commands to supplement the art tools include "magnify," "show picture," and "change colors." To modify existing parts of a picture, the program provides "undo," "cut and paste," "invert colors," and other edit commands. PC Paint includes font commands to set the type style and size of text and file commands to handle entire picture files.

Pictures can be printed on a dot-matrix or color ink-jet printer through the standard "screen dump" interface. Picture files are fully compatible with the Poloroid Palette for color slides or print photography.

PC Paint is supported by the company's PC Mouse, an optical mouse bundled with Designer Pop-up menus for running many of the most popular business application programs for the IBM PC family and compatibles. PC Mouse is now available at a suggested retail price of $195, a $100 reduction. PC Paint also works with any mouse supplied with a Microsoft-compatible driver, including the Microsoft Mouse.

The suggested retail price of PC Paint is $99. The package has been bundled with PC Mouse for an introductory price of $220.

Reader Service Number 6

TI offers voice mail on local area networks

Texas Instruments' Ethervoice is a new software product that provides "voice mail" capabilities for TI Professional Computers in local area networks. The latest addition to the company's Etherseries network products, Ethervoice operates in conjunction with the Ethermail electronic mail module and TI's Speech Command system.

With Ethervoice, TI says, an individual can send voice messages simultaneously to any number of users on the network, without having to enter the message from the keyboard. Ethervoice can be used either for voice message mail or to support text messages. For example, a user can record a voice message and send it for the recipient to play back at his or her convenience. Or a user can attach a voice message to a text message and send them both via Ethermail, allowing important parts of messages to be clarified or emphasized vocally.

Controlled by function keys on the TI Professional Computer keyboard, Ethervoice provides a voice recorder that records voices in two modes—high quality (9600 bits per second) and normal quality (2400 bps).

To implement Ethervoice, a local area network requires a network server (TI Professional Computer) with 256K random access memory, hard disk storage, Etherlink hardware, and Ethershare, Ethermail, and Ethervoice software. Each TI Professional Computer using Ethervoice requires 256K, Etherlink hardware, Speech Command hardware, Speech Command software, and Ethershare user software. Only one copy of Ethervoice is necessary for a typical local area network, since user computers access Ethervoice as needed from the network server.

Ethervoice is priced at $150.

Reader Service Number 7

Board for IBM PC reads/writes Apple disks

Vertex Systems' Apple-Turnover, a board for the IBM PC, allows direct transfer of files between Apple disks and IBM disks.

According to Vertex, the file-copying process is fast and simple. The Appledos 3.3 or Apple CP/M disk is directly inserted into the IBM's disk drive. Individual Apple or IBM disk files, or an entire disk, can be copied. In addition, blank disks can be initialized (formatted) within the IBM for the Apple. Serial-file transfers and modems are eliminated.

The Apple-Turnover software, with features similar to the company's Xeno-Copy family of software utilities, is fully menu-driven and easy to use, says Vertex.

The package contains a half-sized printed-circuit board, disk drive attachment cable, file-transfer software, and a test disk. The Apple-Turnover board is installed in any expansion slot, between the regular disk controller card and the normal IBM disk drives. An Apple test disk is provided to assure proper installation and operation.

Apple-Turnover runs on the IBM PC, XT, and most PC-compatible computers under MS-DOS (PC-DOS). It requires 128K of memory and two disk drives (most hard disk systems are supported).

The price of Apple-Turnover is $279.50.

Reader Service Number 8

Motorola debuts VME-bus-compatible board

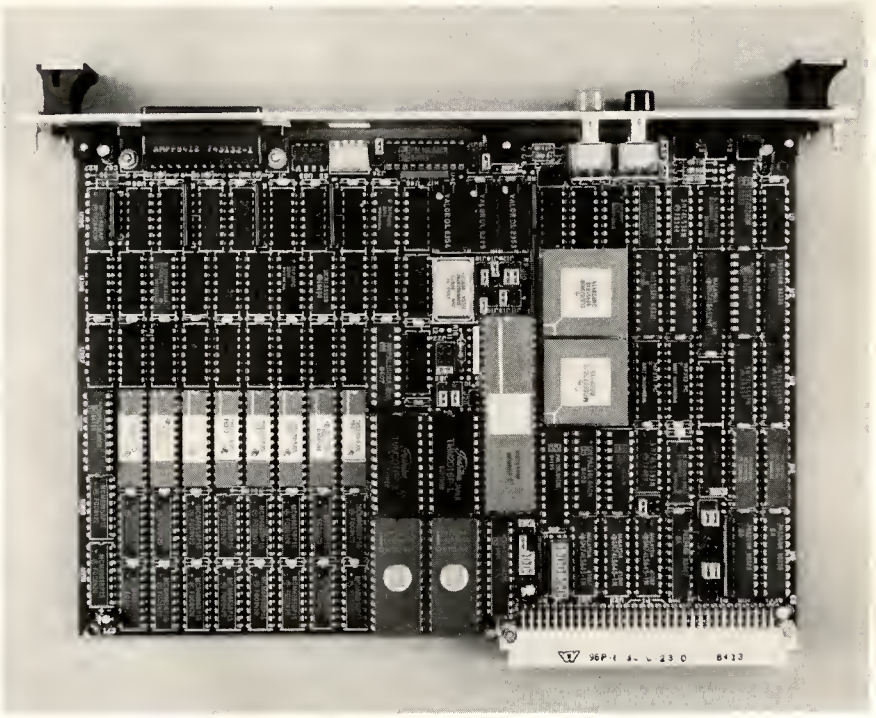
A VME-bus-compatible microprocessor board designed for high-speed image-processing, communications, and industrial control applications has been introduced by Motorola, along with a companion system controller module and an I/O transition board. The MC68010-based MPU board provides a 4K-byte associative memory, or cache, for faster program execution, dual-port dynamic RAM for reduced bus loading with increased execution speed, and the enhanced 68010 instruction set for improved loop execution.

The design of the MPU board (model number MVME120) is optimized for multiprocessor applications. The combination of the MC68010 MPU, the MC68451 memory management unit, and the no-wait-state instruction cache, is, Motorola says, a design highly suited for multiprocessor systems. Such mainframe computer features as virtual machine, virtual I/O, and virtual memory (a key requirement for the Unix operating system) can be implemented on an international-standard microcomputer system bus.

The MVME120's 128K-byte on-board RAM and private ROM can work in parallel with other processors on the same bus, eliminating unnecessary bus loading. The RAM array is dual-ported between the MC68010 MPU and the VME bus to promote efficient communication between cooperating processors. The board is also available with a 512K-byte RAM (model number MVME121).

The companion system controller module MVME050 provides a combination of system control, system utility, and debug/diagnostic functions. It is designed to implement multiprocessing system functions required only once—for example, bus arbitration, bus time-out, system clock generation, and time-of-day clock. Removing these functions from the processor module frees up valuable space and eliminates duplication of system control functions on each processor in a multiprocessor system. Eight 28-pin memory sockets on the system controller module can be used to provide system RAM for common data structures such as semaphores or job queues, system EPROM for common test routines or boot loaders, or a combination of both.

A companion to the system controller board, the I/O transition module MVME701 is an optional, Eurocard-format, double-high board, which is interconnected to the system controller by a ribbon cable. It provides industry standard connectors to external devices for the system controller's serial and parallel I/O ports, along with optional batteries for backup of the time-of-day clock. There are no active components on the VME701 board.



Motorola's MVME120 module includes the 10-MHz MC68010 MPU, a 4K-byte instruction cache, the MC68451 memory management unit, the A24, D16 VME bus interface, a seven-level interrupt handler, four on-board timers, an RS-232C debug terminal port, local abort and reset switches, and three status display LEDs.

The MVME120 MPU board is fully supported by the Versados real-time operating system, release 4.4, scheduled to be available in the first quarter of 1985. In addition, the System V/68 operating system is being ported to the 512K-byte RAM version of this board —also planned for first quarter 1985. System V/68 is derived from, and functionally equivalent to, the Unix System V operating system developed by AT&T Bell Laboratories. A debug/monitor firmware package, the MVME120bug, is optionally available for use with the processor board.

The VMEmodule products are offered at the following prices: MVME120 with 128K-byte RAM, $2575; MVME121 with 512K-byte RAM, $4185; MVME050 system controller module, $1595; MVME701 I/O transition board, $215; MVME120bug debug/monitor firmware, $500. OEM quantity discount pricing is also available.

Reader Service Number 9

Intel's 512K EPROM features page-addressing scheme

Intel's 27513, a member of the company's 512K-bit family of ultraviolet EPROMs, employs a page-addressing scheme to bring high memory capacity to systems based on 8- and 16-bit microcontrollers and 8-bit microprocessors.

The 27513 is partitioned into four 16K-byte pages, reducing the number of address lines needed. This frees the processor's address space for additional EPROM, RAM, or other memory types.

The page-addressing capability of the 27513 thus extends the life of microcomputer systems based on 128K-bit EPROMs. For instance, the 27513 can be substituted for a 128K EPROM in 8-bit systems, quadrupling storage capacity with little or no hardware modification.

The other member of Intel's 512K EPROM family, the 27512, uses the conventional addressing method.

The new EPROMs provide high-density firmware storage for a wide range of applications, saving circuit-board space by allowing more storage to be accommodated by a standard 28-pin socket.

Both EPROMs take advantage of Intel's intelligent programming algorithm, which speeds programming of the chips—typical programming time is less than six minutes, Intel says.

Each EPROM comes in two speed versions, with access times of 250 or 300 nanoseconds. Both offer low power consumption (maximum supply currents of 125 milliamperes active and 40 milliamperes standby) and measure 242 square mils (185 mils by 317 mils).

The price for the 300-ns versions of the 27512 and 27513 is $140 in quantities of 1000, available eight weeks after receipt of order.

Reader Service Number 10

Midrange Eurocard/DIN-based 16-bit bus structure announced

Gespac, Inc., has formally introduced the G-64 microcomputer system bus in the US. G-64 is a Eurocard/DIN-based, second-generation, 16-bit bus for midrange applications, according to the company.

There has been a recent evolution in board-level microcomputer products towards second-generation designs built using the Eurocard form factor with DIN connectors, says Gespac. Several standards have emerged, the company notes, all of them on large and expensive double-height Eurocards and all targeted at the high end of the market. This has created a gap—for a small, inexpensive Eurocard for lower-end and cost-sensitive applications, Gespac asserts.

The company's G-64 bus and its associated boards are designed to fill that gap. The G-64 is a processor-independent, nonmultiplexed, 16-bit bus. It operates in synchronous or asynchronous mode, depending on the microprocessor used.

The G-64's true 16-bit data bus scheme allows high-speed data transfers at up to 2 MHz. Its nonmultiplexed address lines allow direct linear access to up to 512K bytes of memory. It provides a separate memory map of up to 2K bytes for accessing peripheral devices.

The G-64 is a single-processor bus. However, it supports DMA from several cards in a daisy-chain configuration. It has three interrupt levels and an interrupt acknowledge line supporting vectored interrupts. The G-64's power supply lines deliver 5V and ground, plus and minus 12V, and 5V standby. This last line is used to power any CMOS devices that need to remain powered during a general power failure.

Gespac views its 16-bit G-64 bus as the natural replacement for the 8-bit STD bus. The G-64's single-height Eurocard is 100 by 160 mm (approximately 3.9 by 6.25 inches)—or 15 percent smaller than the STD bus card. Its DIN 41612 pin-in-socket connector is far more reliable than an exposed-edge connector, says Gespac, especially in demanding industrial environments.

The following processors are presently supported on the G-64 bus: 6800, 6809, 68008, 68000, 8085, 8088, Z80, 16032, 9995, and J-11. Over 400 products from several manufacturers worldwide are available on the bus and Gespac itself supports the bus with over 85 products. The average selling price of a G-64 Eurocard is around $360.

A 50-page specification manual for the G-64 bus is available free of charge from Gespac.

Reader Service Number 11

AI system offers Smalltalk and interactive graphics

According to Tektronix, its 4404 Artificial Intelligence System, listed at $14,950, offers high performance at a cost well below the price range of existing AI machines. Designed to support AI research and development and to provide a development system for AI-based software products, the 4404 provides the user with an exploratory programming environment that includes a powerful microprocessor, mass storage, an interactive user interface employing a mouse and bit-mapped graphics, and optional networking capability.

The system comes with Xerox's Smalltalk-80 programming language. Tektronix says that its method of implementing Smalltalk-80, combined with the 4404's powerful hardware architecture, achieves execution speeds exceeded only by systems costing over $100,000. Responsive enough to perform on-screen animation, the 4404 makes the Smalltalk graphics interface available as a tool for AI researchers.

The standard 4404 is a desktop system running Smalltalk-80 on the Motorola 68010 processor at 10 MHz with no wait states. A hardware accelerator supports floating-point operations. User memory is 1M byte of RAM, expandable to 2M bytes. Page-on-demand memory management provides a large, 8M-byte virtual-memory address space, permitting development of complex programs without segmentation or overlays. The mass storage system consists of a 20M-byte hard disk and a single 5¼-inch floppy disk. A 40M-byte hard disk with a streaming tape drive is optional.

The 4404's 13-inch monochrome, bit-mapped graphics display operates at 60 Hz, noninterlaced. The 640×480-pixel display acts as a window into the 1024×1024 display address space, with smooth panning over the entire display space.

The system comes with a Centronics-style parallel interface, RS-232, and a Small Computer Standard Interface (SCSI) for connection to host computers, hard-copy devices, and other peripherals. An ANSI-X3.64-compatible terminal emulator allows immediate access to existing computers. Networking capability will be available through an optional Ethernet interface in spring 1985.

The 4404 Artificial Intelligence System from Tektronix is designed to increase productivity in many areas of AI research and development, including expert systems, natural languages, intelligent robotics, vision systems, automatic programming, and theorem proving.

Optional languages include Franz Lisp and Prolog. Franz Lisp is a widely used member of the Lisp family, which has been the primary AI programming language for over two decades. Prolog is popular with European AI researchers and has been selected as the language of the Japanese Fifth-Generation Project.

The Smalltalk-80 language, says Tektronix, offers the advantages of a highly integrated exploration and development environment with an excellent user interface. The object-oriented language simplifies the task of creating large, complex systems by allowing the programmer to defer many constraints and commitments until an overall framework has been defined, working instead with symbolic descriptions of objects. The concepts of classes, objects, and messages are supported directly, and an inheritance mechanism speeds programming and reduces errors. Routines can be executed immediately upon definition, encouraging learning-by-trial approaches to problem solving. The language is highly extensible and makes its internal definitions available to the user through its windowing mechanism.

The 4404 Artificial Intelligence System will be available in January 1985.

Reader Service Number 12

Hardware/software makes PC/XT a publishing workstation

The Concept 100 system from Concept Technologies converts an IBM PC/XT into a full-function, high-performance workstation for business and technical documentation. Users can create high-resolution text and graphics interactively, lay out pages in different formats, and make changes. In addition, the system reproduces the screen image on a printer or other output device at the maximum resolution of the output device.

The capabilities of the Concept 100 are based on a personal computer and hence are not limited by other users' demands on a firm's minicomputer or mainframe system. Yet users still can take advantage of the corporate mainframe and its resident graphics applications. They can load graphics down from the mainframe as needed. Concept 100 accepts mainframe graphics in the Tektronix Plot 10 format and handles computer-aided design files in the CADAM format.

The Concept 100 uses an Intel 80186-based intelligent graphics subsystem board, which provides fast, interactive display; background graphics printing on dot matrix and laser printers; and an enhanced user interface for graphics input via a mouse. This subsystem replaces and emulates IBM monochrome and color display adapters and accelerates the speed of Virtual Device Interface (VDI) graphics. Existing software for the IBM PC/XT will run on the system.

A high-resolution screen allows the display of high-quality text and graphics, says the company. Two levels of intensity for both alphanumerics and graphics are provided. The 720×352 display is 50 Hz, noninterlaced, and it supports 25 rows and 80 columns of characters.

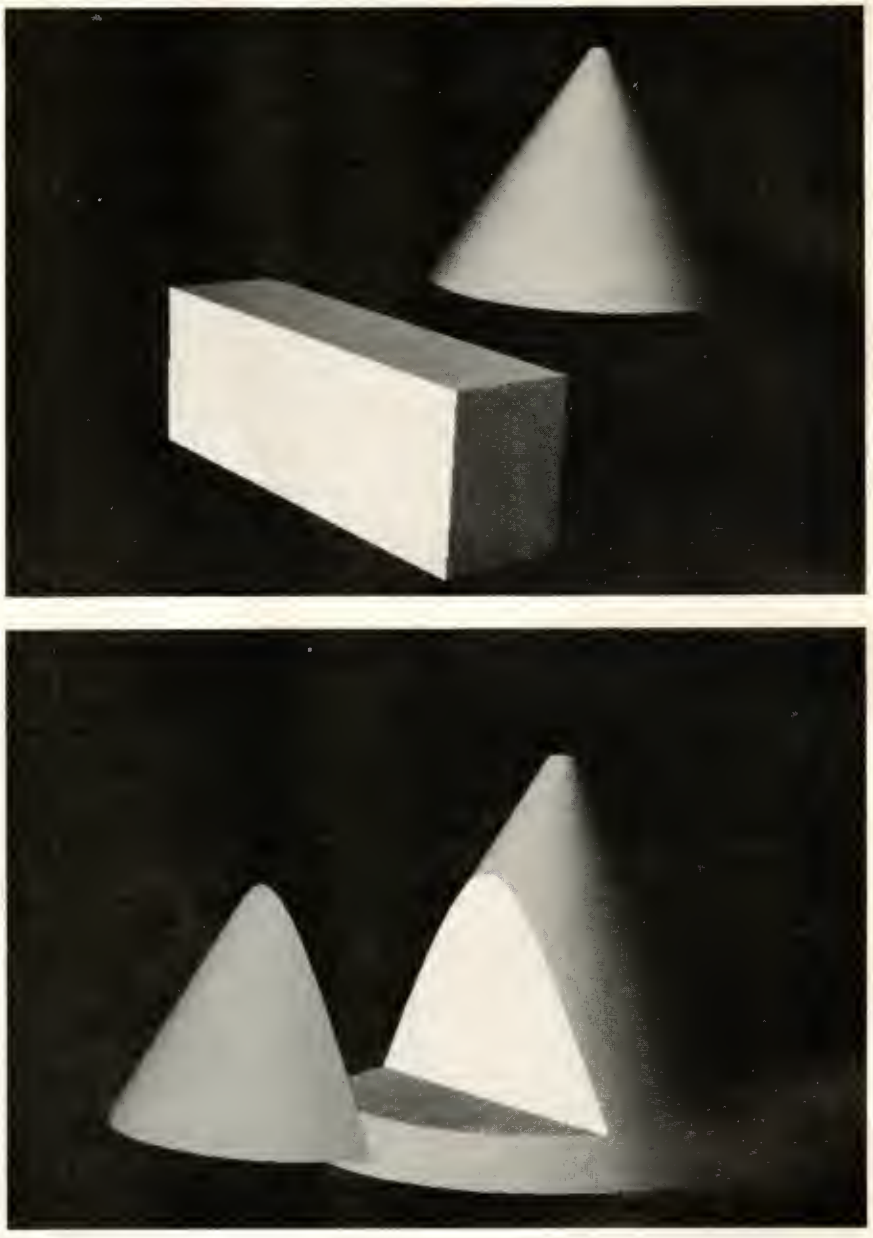
The system supports many popular printers, such as the Epson FX80 and MX100, the IBM graphics printer, the Hewlett-Packard Thinkjet, and the IDS P series. Centronix parallel and RS-232C serial ports are offered.

Concept 100 supports the Mouse Systems mouse and the Xerox optical mouse. It also supports the IBM monochrome display and the PGS Max 12 monitor.

The workstation's graphics editor makes available many of the drawing capabilities of a computer-aided design package, such as zoom and pan, cross-hatching, and color output. The system lets users create complex organizational charts, schedules, flow diagrams, and block diagrams. It creates text, lines, boxes, circles, and polygons, and can produce graphs, maps, and text with diagrams. It allows nonprogramming users to create overhead presentations with simple commands and menus. According to Concept Technologies, users can learn to use the graphics editor in about 30 minutes, and even infrequent users can produce presentation output within a few minutes.

The Concept 100 system includes the graphics subsystem, mouse, disk-based software, and documentation. It is priced at $2195 and is delivered 45 days after receipt of the order.

Reader Service Number 13



In this example of an intersection operation performed by means of Cubicomp's Boolean extension of its solid modeling system for the IBM PC, the box has intersected the cone to form a new image. These images were constructed in less than a minute, the company says.

Cubicomp adds Boolean operations to solid modeling system

Cubicomp Corporation has added a Boolean construction operations extension to its microcomputer-based solid modeling system. The new extension permits industrial designers and other CAD users to simulate the fabrication process that transforms raw material into a finished product. Cubicomp believes it is the first to offer Boolean operations on a microcomputer, creating a low-cost CAD system that competes with minicomputer-based systems.

Boolean construction operations allow the user to relate two objects in three different ways—union, intersection, and subtraction. These operations can depict such procedures as sawing cuts, drilling holes, and joining flat and curved objects. For example, the union of a cylinder and a cube shows the cylinder slicing through the cube. The intersection operation depicts only the part of the cylinder that intersects the cube. And the subtraction of the cylinder from the cube yields a cylindrical hole drilled through the cube.

The Cubicomp solid modeling system is based on the IBM Personal Computer (and compatibles) and permits users to create, display, manipulate, and store three-dimensional, full-color, shaded-surface solid models. The system displays up to 4096 colors out of a palette of 16.8 million.

The Boolean construction operations module is priced at $1900.

Reader Service Number 14

Software speeds ladder documenting for process control

Sumicom, Inc., has announced the availability of the PCD-200 Ladder Documentator software program for editing and documenting ladder diagrams in process control applications. Ladder Documentator, developed by Indelec, Inc., is specifically designed for the Sumicom System 830 desktop microcomputer.

The program, with its full, on-screen editing capabilities, reduces time and costs spent documenting ladder diagrams, Sumicom says. Since the standard language of over 90 percent of programmable controller applications is the relay ladder diagram, these savings can be significant.

According to Sumicom, the PCD-200 software eliminates two problems historically encountered by the process control industry. The first is the inability to retrieve up-to-date ladder documentation contained in the programmable controller's memory for corrective function block programming. The second is time-consuming cross-referencing, when data is available, from numerical to alphanumeric designations of elements within the system.

With the PCD-200, data from the programmable controller can be viewed at any time; the user can view the ladder listing in part or in its entirety, inserting changes, corrections, and comments as desired. In both cases, information can be displayed on the System 830's CRT screen, printed on the internal dot matrix printer or reproduced in up to eight colors on an optional plotter, and output for storage to a floppy or hard disk peripheral. With the ability to search for any item or sequence of items, users can easily incorporate changes, even when a single item appears dozens of times in a diagram, thereby assuring complete correction of the program.

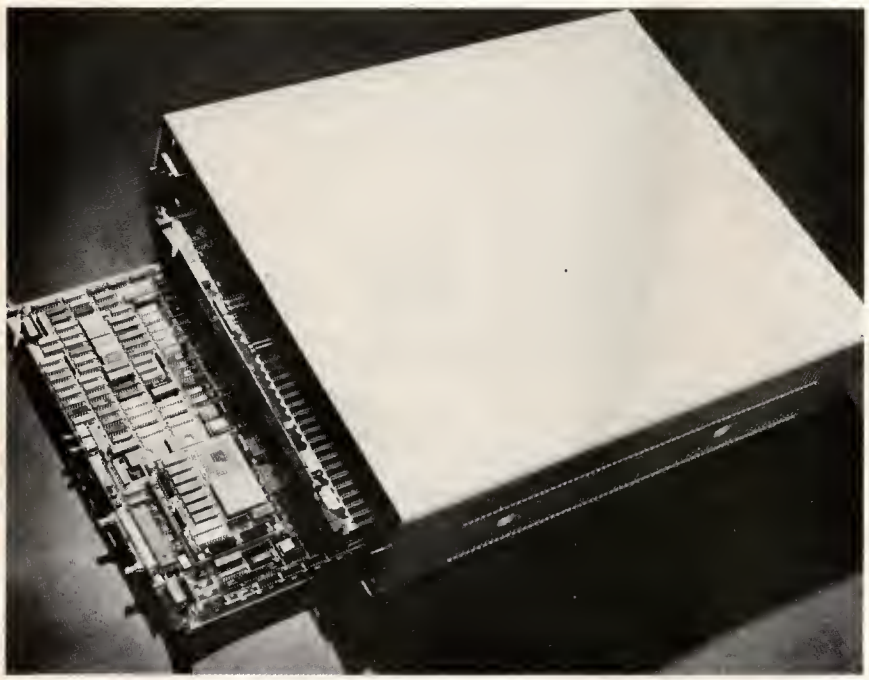
The PCD-200 also allows for selective output generation from start rung (network) to end rung or from start contact number (coil number) to end contact number.

Additionally, the software program offers users a cumulative error-listing summary, an input/output uage listing, and on-screen search for individual symbols and displays.

The software is available for use with Allen-Bradley, Gould-Modicon, Texas Instruments, and General Electric controllers.

The basic Sumicom System 830 microprocessor configuration includes processor, printer, keyboard, color CRT, RS-232 interface, two 1M-byte disk drives, and operating software in a self-contained unit for a suggested retail price of $3995. The PCD-200 Ladder Documentator software is $995.

Reader Service Number 15



Motorola's Benchmark 20 package for MC68020 monitoring and code debugging includes the VM13 1M-byte DRAM board, the 020bug firmware package for software checkout, and the VM04 Monoboard Microcomputer with MC68020 MPU, 4K-byte instruction cache, and hardware memory management unit.

System provides tools for MC68020 code development

Benchmark 20, a 32-bit system that gives first-time MC68020 users software tools to evaluate and start code development for the chip, has been announced by Motorola Microsystems. The system provides tools for benchmarking and code debugging, paged memory management, and Versamodule compatibility that allows configuration with other Versamodule boards.

The Benchmark 20 package, used with an appropriate software development host, features the MC68020-based VM04 Monoboard Microcomputer, the VM13 dual-ported Versamodule 1M-byte dynamic RAM board, a four-slot chassis with power supply, and 020bug firmware. Software can be assembled or compiled on a Motorola VME/10 or Exormacs host system, then downloaded for execution into the Benchmark 20.

The 020bug, EPROM resident on the VM04, allows the user access to VM04 resources including any MC68020 internal register, VM04 status/control bits, timer for benchmarking applications, and any memory-mapped Versabus or Rambus resource. In addition to these user utilities, 020bug provides two types of power-up self-test diagnostics; software drivers to accommodate both serial ports, including download and upload capability from a host computer; an operating system bootstrap command; and breakpoint and trace modes for program debug development.

Benchmark 20 is priced at $14,995.

Reader Service Number 16

Information service covers personal computer peripherals

Future Computing Incorporated, an information services firm devoted to the personal computer industry, has announced Peripherals 85, a comprehensive service that examines market and technical issues affecting personal computer peripherals.

The Peripherals 85 portfolio includes four reports:

"Distribution Channels" analyzes key relationships of major personal computer industry participants and their suppliers. It includes case studies of the distribution policies of major peripherals companies.

"Printers and Plotters" covers the major categories of printers and plotters and their application areas. Software and compatibility issues are also discussed.

"Mass Storage Devices and Media" contains profiles of top producers of flexible and hard disk drives, tape systems, and magnetic media serving personal computers. It includes market forecasts, analyzes distribution channels, and discusses strategies for selling to the retail channel.

"Add-in Boards, Modems, Monitors, & Input/Output Devices" analyzes the markets for these products and describes leading manufacturers, personal computer configurations, and corresponding market opportunities.

In addition to the four reports, the service includes subscriptions to *FutureViews* and one other Future Computing newsletter.

Peripherals 85 includes 20 hours of access to Future Computing's inquiry service. Subscribers may use the service to ask about trends and developments in any segment of the personal computer industry.

The price of the Peripherals 85 service is $15,000.

Reader Service Number 17

The Product Summary is a review of selected product announcements received at *IEEE Micro*'s offices during the last two months. For information on any of these products, circle the appropriate Reader Service Number on the card at the back of the magazine.

IEEE MICRO'S PRODUCT SUMMARY

Product Summary Editor: Victor P. Nelson

MANUFACTURER & MODEL	FUNCTION	COMMENTS	R.S. NO.
CHIPS/COMPONENTS			
Motorola, MCM2833	32K EEPROM	Operates from a single +5V power supply in the read, write, and erase mode and offers word erase and write controlled by TTL signal levels. 4096 × 8-bit device comes in 150- and 200-ns versions; 28-pin. $23.30 in 100's.	30
Telmos, TML1840	8-bit video DAC	Silicon-gate, 25-MHz, 100-mW device drives 75-ohm cable directly, with the full-scale output current adjustable via an external resistor. Has composite sync, composite blank, and 10-percent bright. Provides linearity of one LSB; will accept TTL or CMOS inputs. 24-pin CERDIP is $26.60 in 100's.	31
VLSI Technology, VL4500A	DRAM controller	Alternate-source version of TMS4500A operates at 150 ns, directly drives up to 256K bytes of 64K dynamic RAM, and provides address multiplexing, refresh control, and time control. Operates from the microprocessor clock. 40-pin plastic DIP is under $10 in volume.	32
Texas Instruments, TIBPAL16XX series	Programmable array logic	Four PAL devices operate with propagation delays of 15 nanoseconds maximum (10 ns typical) and at maximum output-register toggle frequencies of 50 MHz. According to TI, devices are suitable for use as high-speed, data-path-logic replacements. Require current of 180 mA maximum. 20-pin plastic DIPs are $5.18 each in 25,000-piece quantities.	33
Advanced Micro Devices, Am7990/7992A	Ethernet chip set	Am7990 LAN controller and Am7992A serial interface adapter support 10M-bit-per-second networking applications; are compatible with IEEE 802.3. The chips' 16-bit bus interface is compatible with the iAPX 86, the 68000, the Z8000, and the LSI-11 microprocessor families. Packaged in a 48-pin CERDIP, the 7990 is $76.50 in 100's; the 24-pin 7992A, in a SLIMDIP ceramic package, is $23 in 100's.	34
Motorola, MC68HC11	Microcomputer chip	M6801-family-compatible device is designed to run at a 2-MHz bus speed across a −40 to +125°C temperature range. Features 3V to 5.5V operation, STOP and WAIT modes, 8K bytes of ROM, 512 bytes of EEPROM, 256 bytes of static RAM, an 8-bit pulse accumulator circuit, and an 8-channel, 8-bit A/D converter. Under $20 each in volume quantities.	35

For more information, circle the appropriate RS No. on the Reader Service Card at the back of the magazine.

MANUFACTURER & MODEL	FUNCTION	COMMENTS	R.S. NO.
BOARDS			
Gespac, GESMPU-8	Single-board computer	8088-based single-height Eurocard is compatible with the G-64 bus. Provides a socket for an 8087 arithmetic coprocessor and a socket for up to 32K bytes of EPROM; also provides 2K bytes of CMOS RAM and an RS-232C synchronous or asynchronous serial interface with a programmable baud-rate generator. $495.	36
Motorola, VM04	Single-board computer	Based on an MC68020 MPU operating at a fixed clock of 16.67 MHz, Versabus-compatible board provides memory management, an on-board cache designed to complement the on-chip instruction cache, and dual multiprotocol serial I/O ports. Intended for use with VM13 1M-byte memory board. $6855 in quantity 1-5 (VM13 is $4200 in quantity 1-5).	37
SYSTEMS			
Compupro, System 816/G	Microcomputer system	IEEE 696/S-100-compatible, 32-bit system uses the 6-MHz NS32016 CPU, the NS32082 MMU, and the NS32081 floating-point unit. Features 1M bytes of static RAM (expandable to 16M bytes), 2M bytes of solid-state disk memory, 12 serial ports, one printer port, and one parallel port. With a 2.4M-byte dual 8-inch floppy subsystem, price is $17,495. Hard disks of up to 80M bytes can be added.	38
Cromemco, System 100 and 300 series	Microcomputer systems	Systems use Unix System V with the Berkeley enhancements. Can accommodate up to 16 users and feature a 10-MHz 68000, up to 16M bytes of error-correcting RAM, cache memory for disk operations, a 50M-byte hard disk, and 2 to 14 open slots. Prices start at $9995.	39
Applied Computer Techniques, Apricot Portable	Portable microcomputer system	8086-based machine incorporates voice recognition, a 25-line × 80-column (640 × 256-pixel) LCD display, 256K RAM (expandable to 1M bytes), a 720K double-sided 3.5-inch disk drive, and an infrared keyboard and infrared mouse/trackball in a 13-pound package. It includes bundled executive, graphics, and system software. $2695.	40
MISCELLANEOUS			
Avocado Computer, Grayscaler	Color card converter	Upgrades any IBM PC or PC-compatible color graphics card to true gray-scale operation. Provides 16 brightness levels of composite video; is driven from RGB port. According to company, adapter aliminates the color "grain" caused by operating directly from a color card and is software-transparent. $59.95.	41
Winterhalter, Inc., Datatalker/MAC	3270 emulator	Intelligent front-end data communications processor allows the Apple Macintosh to emulate IBM 3271/3277, 3274/3278, 3275, and 3276/3278 interactive terminal systems. Supports all 3270 function keys. Communications features include transfer rates of up to 9600 baud, half- or full-duplex operation, multidrop or point-to-point network links, and a synchronous RS-232C interface. Unit, software, cable, and manual are $1095.	42

For more information, circle the appropriate RS No. on the Reader Service Card at the back of the magazine.

MANUFACTURER & MODEL	FUNCTION	COMMENTS	R.S. NO.
Digital Equipment Corp., Pro/Venix	Operating system	Multitasking, multiuser operating system for the Professional Series of personal PDP-11 computers is based on Version 7 of AT&T Unix and includes the more popular of the Berkeley enhancements. It is distributed with an AT&T Technologies System V license so that upgrades to newer releases of AT&T Unix can be accommodated. Includes a complete software development environment. $800.	43
C. Itoh Digital Products, Inc., PC Itoh Utilities	Printer driver software	Allows IBM PC users to print spreadsheet graphs in color, run software written for other printers, and create custom character sets on eight of C. Itoh's Prowriter Model 8510/1550 dot-matrix printers. Includes a Lotus 1-2-3 color interface. Ten-program package is $55.	44
Integrex Ltd., Colourjet 132	Color printer	36-color ink-jet printer is IBM-PC-compatible; provides up to 252-dot-per-inch resolution. Features include double-width, double-height, and double-size printing as well as underlining, italics, programmable fore- and background colors, and 80-column or 132-column-compressed output. The unit can also print in full videotext format from a Centronics parallel input. $795.	45
Intelligent Technologies, Bisync Exchange series	3270, 3780 emulators	Bisync Exchange 3270 enables an IBM PC to emulate an IBM 3274/6 cluster controller, an IBM 3278/9 terminal, and an IBM 3287 printer. Bisync Exchange 3780 enables a PC to emulate an IBM 3780 or 2780 terminal, thus allowing users to upload and download files between their PCs and a host mainframe. Packages are $795 and $695, respectively.	46
Sysgen, Inc., SC4500 series	Tape controllers	OEM units for the IBM PC, PC/XT, and compatibles control either a 10M-byte streaming cassette drive or a 20M- or 45M-byte streaming quarter-inch cartridge drive. Offer verification on-the-fly and both mirror-image and streaming file-by-file backup; use the QIC-36 interface. $295.	47
Sophia Systems, SA700 family	In-circuit emulator systems	Emulators for 8- and 16-bit microprocessors include integrated CRT, ASCII keyboard, 8-inch floppy-disk drive, PROM programmer, logic-state analysis probes, and in-circuit emulator. Provide full symbolic debugging capability independent of a host development system; can read executable object files from systems such as Intel's MDS Series II and III, iRMX-86, CP/M-86, and CP/M 2.2. Prices are under $10,000.	48
Connecticut Microcomputer, Inc., GPAD-C	Printer adapter	Allows any printer with a Centronics printer interface to be connected to any computer or controller with an IEEE 488 interface. The computers and controllers supported include those made by Hewlett-Packard, Tektronix, Commodore, and Osborne. Unit comes with two cables and a power supply; sells for $179.	49
Datel, Passport SDAS-8	Data acquisition system	Accepts 8 differential analog channels and transmits them as ASCII serial data to a host computer or terminal via simple command characters. Inclusion of both asynchronous RS-232C and isolated current-loop serial I/O enables the unit to be remotely located so that the host computer is not exposed to factory conditions. May be connected to the serial port of any IBM PC, Apple, or TRS-80 personal computer. $395.	50

For more information, circle the appropriate RS No. on the Reader Service Card at the back of the magazine.

ACCESS

recent books and articles on microcomputing

by Peter R. Rony
Dept. of Chemical Engineering
University of Delaware
Newark, DE 19716

Articles

Business Computer Systems

Vol. 3, No. 6, June 1984:

A. Bernstein, "Defining Integrated Software," pp. 56-82.

K. Mayo, "A Closer Look at Monitors," pp. 84-100.

E. Horwitt, "Looking for the Promised LAN," pp. 112-148.

Vol. 3, No. 7, July 1984:

H. Swartz, "The Software Buyer: Owner or Licensee?" pp. 17-20.

D. Post, "General Ledger's Bottom Line" [general ledger software], pp. 68-93.

T. Woods, "The Laser Factor," pp. 96-100.

A. Bernstein, "UPSmanship" [uninterruptible power supplies], pp. 105-118.

Vol. 3, No. 8, Aug. 1984:

H. Swartz, "A Lemon Law for Computers?" pp. 22-23.

A. Bernstein, "Desktop Networks: Off the Drawing Board," pp. 34-45.

L. Li and S. Austin, "Ready When You Are" [briefcase-size computers], pp. 49-58.

T. C. Dulaney, "Shape Up, Ship Out" [traffic and distribution programs], pp. 60-80.

D. Post, "Striking a Balance" [finance and accounting software], pp. 92-122.

Byte

Vol. 9, No. 7, July 1984:

R. Jadrnicek, "Symphony: A Full-Orchestra Version of Lotus 1-2-3," pp. 121-123, 372-373.

S. H. Saib, "An Ada Language Primer: Part 2," pp. 139-141, 386-397.

F. da Cruz and B. Catchings, "Kermit: A File-Transfer Protocol for Universities: Part 2—States and Transitions, Heuristic Rules, and Examples," pp. 143-145, 400-403.

Special report on computers and video. Articles include: "Electronic Encyclopedias," "Televisions as Monitors," Computer Control of a Video Recorder," "Videodiscs and Computers," and "Controlling Videodiscs With Micros," pp. 149-228.

Reviews on the Sage II and Sage IV computers, the Compaq Plus, Xenix for the IBM PC/XT, Turbo Pascal, Lisp for the IBM PC, and the Smith-Corona L-1000 printer, pp. 233-297.

Communications of the ACM

Vol. 27, No. 6, June 1984:

L. Fujitani, "Laser Optical Disk: The Coming Revolution in On-Line Storage," pp. 546-554.

Computer

Vol. 17, No. 8, Aug. 1984:

Special issue on fault-tolerant computing. Articles include "Architecture of Fault-Tolerant Computers," "Fault-Tolerant Systems in Commercial Applications," "Designing for Ultrahigh Availability: The Unix RTR Operating System," "The Intel 432: A VLSI Architecture for Fault-Tolerant Computer Systems," "Fault-Tolerant Semiconductor Memories," "Autonomous Decentralized Computer Control Systems," and "Fault Tolerance by Design Diversity: Concepts and Experiments," pp. 6-80.

Computer Design

Vol. 23, No. 7, June 15, 1984:

H. J. Hindin, "Formal Protocol Specification Ready to Make Its Mark," pp. 57-64.

S. Ross and J. MacAllister, "Practical and Continuous Speech Recognition," pp. 69-76.

Part II of a special report on microprocessors and microcomputers. Articles include "Thirty-Two Bit Micros Power Workstations," "Message Passing Supports Multiple Processor Design," "Bus Structure Eases Multiprocessor Integration," "Versatile Bus Suits Real-Time Processor Applications," "Portable Native Code Package Suits 8- to 32-bit Micros," and "Using Personal Workstations for Software Development," pp. 95-161.

Data Communications

Vol. 13, No. 8, July 1984:

W. Sapronov, "Gateways Link Long-Haul and Local Networks," pp. 111-122.

S. Joshi and V. Iyer, "New Standards for Local Networks Push Upper Limits for Lightwave Data," pp. 127-138.

E. G. Brohm, "Sampling New Technologies of Network Processors," pp. 143-147.

R. H. Swanson, "Primer: Satellite Communications for Managers," pp. 151-157.

G. Held, "Standards Would Reduce Cost of Async Micro Communications," pp. 161-168.

E. Lucier, "Putting a Price on File Transfer," pp. 177-187.

Books

Engineering Research Associates, Inc., "High-Speed Computing Devices" (Volume 4 in the Charles Babbage Institute Reprint Series for the History of Computing), The MIT Press, 1984, 451 pp., $38.00.

P. Freiberger and M. Swaine, "Fire in the Valley," Osborne/McGraw-Hill, 1984, 288 pp., $9.95.

A. Veronis, "Microprocessors: Hardware and Applications," Reston Publishing Co., Inc., 1984, 928 pp., $34.95.

M. V. Wilkes, D. J. Wheeler, and S. Gill, "The Preparation of Programs for an Electronic Digital Computer" (Volume 1 in the Charles Babbage Institute Reprint Series for the History of Computing), The MIT Press, 1984, 167 pp., $30.00.

Datamation

Vol. 30, No. 10, July 1, 1984:

G. Troy, "Thwarting the Hackers," pp. 117-128.

Vol. 30, No. 11, July 15, 1984:

I. S. Nesbit, "Evaluating Micro Software," pp. 74-78.

V. Rauzino, "Tying the Micro-Mainframe Knot," pp. 83-90.

K. D. Morse, "Shrinking VMS" [DEC's VAX operating system], pp. 95-100.

D. Livingston, "Computer Conferencing," pp. 111-116.

F. Sweet, "What, If Anything, Is a Relational Database?" pp. 118-124.

T. Guimaraes, "The Evolution of the Information Center," pp. 127-130.

Vol. 30, No. 12, Aug. 1, 1984:

S. Emerson, "The Unix Universe," pp. 76-78.

D. Morris, "How Not to Worry About Unix," pp. 83-86.

D. F. Barlow and N. S. Zimbel, "Unix—How Important Is It?" pp. 90-101.

D. Ferris and J. Cunningham, "Local Nets for Micros," pp. 104-109.

G. M. Pfister, "The PBX: What Matters, What Doesn't," pp. 121-124.

Dr. Dobb's Journal

Vol. 9, No. 7, July 1984:

G. M. Silvey, "Using Resident System Extensions Under CP/M Plus," pp. 36-45.

A. T. Schreiner, "p—A Small-C Preprocessor," pp. 46-82.

S. A. Ruzinski, "A Simple Minimax Algorithm," pp. 84-101.

E. E. Bergman, "Languages and Parentheses (A Suggestion for Forth-Like Languages)," pp. 102-108.

Vol. 9, No. 8, Aug. 1984:

J. Thomas and G. Fletcher, "Scistar—Greek and Math Symbols for Wordstar," pp. 26-29.

D. E. Cortesi, "What's the Diff?—A File Comparator for CP/M Plus," pp. 30-43.

J. A. Thomas and J. Thersites, "Designing a File Encryption System," pp. 44-85.

J. E. Staneff, "A Small-C Concordance Generator," pp. 86-105.

EDN

Vol. 29, No. 1, Jan. 12, 1984:

"*EDN*'s 1983 Technical Article Database," pp. 178-253. [Includes titles of articles from *EDN, Electronic Design, Electronics, Electronic Products,* and *Computer Design.*]

Vol. 29, No. 12, June 14, 1984:

B. Travis, "Special Report: Data Converters," pp. 118-147.

J. Alberkrack, "Switching-Regulator Subsystems Simplify DC/DC-Converter Design," pp. 153-162.

L. Wakeman, "Transmission Line Effects Influence High-Speed CMOS," pp. 171-177.

L. A. Roberts and M. MacDonald, "Use Programmable Logic Chips to Simplify Programmer Design," pp. 217-229.

Vol. 29, No. 13, June 28, 1984:

E. R. Teja, "Winchester Disk Drives," pp. 132-146.

R. H. Cushman, "Additional LSI and Hybrid Parts Ease Completion of LAN," pp. 153-158.

A. Rappaport, "Hands-On Chip Analyses Determine Project Success," pp. 213-218.

J. Haight, "GaAs Logic Characteristics Result in Integration Problems," pp. 225-232.

C. Lee, T. Valentino, and D. Yoder, "Understand System Partitioning to Optimize Custom IC Use," pp. 255-268.

V. K. Agrawal and S. Murugesan, "Algorithm Converts BCD Fractions to Binary," pp. 278-280.

Vol. 29, No. 14, July 12, 1984:

W. Twaddell, "High-Speed CMOS RAMs Score Across Memory Spectrum," pp. 62-68.

P. G. Schreier, "Conditioners Yield Smooth Inputs to Line-Sensitive μC Systems," pp. 218-230.

D. Powers, "Ada-Related Products Abound, But Validation Remains Elusive," pp. 268-276.

Electronic Design

Vol. 32, No. 13, June 28, 1984:

R. Brownstein, "Project Management With Personal Computers," pp. 128-138.

S. Ohr, "Technology Report: Printers," pp. 144-156.

D. Wilburn and J. Mick, "Development Tool Debugs Entire Microcoded Systems Down to VLSI Chips," pp. 169-178.

R. Loughlin and R. Schneider, "Symbolic Database Speeds Debugging of High-Level μP Code," pp. 187-198.

C. MacKenna, "Bus Controller Chip Lets Processor Board Switch Master and Slave Roles," pp. 243-254.

A. Fletcher and R. Mirabella, "Workstation Integrates Design's Two Pillars: The Logical and Physical," pp. 261-276.

M. Alexander, D. Blanchard, and E. R. Abramcyzk, "Depletion-Mode MOSFETs Open a Channel Into Power Switching," pp. 281-286.

J. D. Breemer, "Short Software Routine Quickly Generates Pseudorandom Numbers," p. 296.

H. Winard, "Focus on Switching Power Supplies," pp. 301-312.

Electronics

Vol. 57, No. 13, June 28, 1984:

Special report on computer graphics. Articles include "Computer Graphics," "Pixel Phasing Smoothes Out Jagged Lines," and "A New Generation Video Processor Boosts Resolution," pp. 113-124.

R. Naeini, "A Few Statement Types Adapt C Language to Parallel Processing," pp. 125-129.

R. Cox, "ECL-CML Gate Array Speeds Superminis While Saving Space and Power," pp. 137-140.

Vol. 57, No. 14, July 12, 1984:

F. Ware et al., "Fast 64-Bit Chip Set Gangs Up for Double-Precision Floating-Point Work," pp. 99-107.

J. Theus, M. Taub, and R. V. Balakrishnan, "Futurebus Anticipates Coming Needs," pp. 108-112.

P. Brody, F. Luo, and P. Malmberg, "Active-Matrix Addressing Enhances Flat Panels," pp. 113-117.

S. Eidson, "Leased-Line and Videotex Applications Are Targets of One-Chip Modem," pp. 119-123.

R. Woodcock, "Robot Basic Integrates Functions to Facilitate Off-Line Programming," pp. 124-127.

Electronics Week (formerly **Electronics**)

Vol. 57, No. 15, July 23, 1984:

L. S. White, Jr., G. J. Armstrong, and G. R. M. Rao, "1 MB Memories Demand New Design Choices," pp. 123-126.

Vol. 57, No. 16, July 30, 1984:

J. Lyman, "PC Boards Go Hi-Tech to Meet New Demands," pp. 47-52.

F. Jenne, "CMOS Outstrips Its Competitors in Chip Race," pp. 53-55.

Vol. 57, No. 17, Aug. 6, 1984:

R. Rosenberg and T. E. Feldt, "Local Nets Arrive in Force," pp. 67-73.

J. V. Chatigny, "Piezo Film Yields Novel Transducers," pp. 74-77.

Vol. 57, No. 18, Aug. 13, 1984:

D. M. Weber, "Digital Circuits Point Towards Better TV Sets," pp. 49-58.

M. Hurst, "Evaluating Network Solutions," pp. 60-64.

Vol. 57, No. 19, Aug. 20, 1984:

A. Bindra, "Converters Gain Speed, Resolution," pp. 63-68.

N. L. Kerth, "Software Tools Automate Structured Analyses," pp. 69-72.

Elektor

Vol. 10, No. 6, June 1984:

"ZX Extensions," pp. 6-24 to 6-31.

Hewlett-Packard Journal

Vol. 35, No. 7, July 1984:

S. L. Wechsler, "A New Hand-Held Computer for Technical Professionals," pp. 3-10.

N. Meyers, "Soft Configuration Enhances Flexibility of Hand-Held Computer Memory," pp. 10-13.

J. P. Dickie, "Custom CMOS Architecture for a Hand-Held Computer," pp. 14-17.

T. B. Lindberg, "Packaging the HP-71B Hand-Held Computer," pp. 17-20.

S. M. Blascow, Jr. and J. A. Donnelly, "Module Adds Curve-Fitting and Optimization Capabilities to the HP-71B," pp. 22-24.

L. W. Grodd and C. M. Patton, "ROM Extends Numerical Function Set of Hand-Held Computer," pp. 25-36.

R. M. Miller, "Plug-In Module Adds Forth Language and Assembler to a Hand-Held Computer," pp. 37-40.

Vol. 35, No. 8, Aug. 1984:

S. Sukumar, "Touchscreen Personal Computer Offers Ease of Use and Flexibility," pp. 4-6.

L. E. P. Wood and C. H. Whelan, "Operating System and Firmware of the HP 150 Personal Computer," pp. 6-10.

P. R. Straton, S. R. McClelland, and T. E. Kilbourn, "The HP 150 Touchscreen: An Interactive User Input Device for a Personal Computer," pp. 11-15.

P. S. Showman et al., "Applications Software for the Touchscreen Personal Computer," pp. 15-24.

J. E. Watkins, P. A. Brown, G. Szeman, and S. E. Carrie, "Hardware Design of the HP 150 Personal Computer," pp. 25-30.

J. D. Barbera, "Personal Computer Printer Is User-Installable," pp. 30-31.

IEEE Circuits and Systems Magazine

Vol. 6, No. 2, June 1984:

G. K. Kostopoulos, "Design and Analysis Nomograms for Pulse-Width and Frequency Modulation Using the 555 Timer," pp. 4-11.

IEEE Communications Magazine

Vol. 22, No. 7, July 1984:

M. W. Rahm, "Broadband Network: A User Perspective," pp. 7-10.

C. S. Nokes, "Data Communications and the Large User: The Need for Bridging Systems," pp. 11-17.

Vol. 22, No. 8, Aug. 1984:

C. D. Tsao, "A Local-Area Network Architecture Overview," pp. 7-11.

A. S. Acampora and M. G. Hluchyj, "A New Local-Area Network Architecture Using a Centralized Bus," pp. 12-21.

M. R. Finley, Jr., "Optical Fibers in Local-Area Networks," pp. 22-35.

C. Petitpierre, "Meshed Local Computer Networks," pp. 36-40.

J. O. Limb, "Performance of Local-Area Networks at High Speed," pp. 41-45.

B. W. Stuck, "An Introduction to Traffic Handling Characteristics of Bus Local-Area Network Distributed Access Methods," pp. 46-56.

IEEE Computer Graphics and Applications

Vol. 4, No. 5, May 1984:

J. Yamada, N. Saito, and A. Tamura, "A Low-Cost Drafting System Based on a Personal Computer," pp. 61-65.

IEEE Control Systems Magazine

Vol. 4, No. 3, Aug. 1984:

W. K. N. Anakwa, T. Srinivasan, and B. J. Thomas, "Digital Control of an Unstable Plant," pp. 9-13.

IEEE Design & Test of Computers

Vol. 1, No. 2, May 1984:

J. R. Kuban and W. C. Bruce, "Self-Testing the Motorola MC6804P2," pp. 33-41.

IEEE Spectrum

Vol. 21, No. 7, July 1984:

"Best Bits: Applications of Microprocessors." Topics include "Distributing Among Micros," "Taking Orders," and "Metering Electric Power."

H. S. Watkins and J. S. Moore, "A Survey of Color Graphics Printing," pp. 26-37.

Vol. 21, No. 8, Aug. 1984:

L. A. Zadeh, "Making Computers Think Like People," pp. 26-32.

Vol. 21, No. 9, Sept. 1984:

"Best Bits: Applications of Microprocessors." Topics include "Making Telephones Very Smart," "Controlling Power Plants," and "Digital Data Logging."

F. Guterl, P. Wallich, and M. A. Fischetti, "In Pursuit of the One-Month Chip: Design, Fabrication, Testing, and Business Outlook," pp. 28-49.

IEEE Transactions on Industrial Electronics

Vol. IE-31, No. 3, Aug. 1984:

M. R. Stojic, "Design of the Microprocessor-Based System for DC Motor Speed Control," pp. 243-248.

N. Matsui, T. Takeshita, and M. Yura, "One-Chip Microcomputer-Based Controller for the McMurray Inverter," pp. 249-254.

L. Johansson, H. N. Koivo, and A. Peltomaa, "Design of a Microprocessor Control System for a Solid-Fuel Water Boiler," pp. 263-268.

Infosystems

Vol. 31, No. 7, July 1984:

"CRT Comparison Chart," pp. 100-101.

Interface Age

Vol. 9, No 6, June 1984:

J. M. Allswang, "Buying Japanese?" pp. 36-41.

J. Shepherd, "East Meets West in the Battle for High-Tech Supremacy," pp. 53-56.

R. H. Edelson, "Characters per Second: A Guide to Selecting the Perfect Printer," pp. 59-63.

"Ten Contenders in the Japanese Micro Challenge" [Canon AS-100, Sumicom System 330 and System 830, NEC Advanced Personal Computer, the Fujitsu Micro 16s, Seiko Series 8600, Sanyo MBC 1150, Mitsubishi PC816, and Sord M68], pp. 76-93.

Reviews of the following software are included: Word (Microsoft), Optimum (Uveon Computer Systems), Screen (Basic Business Software), and Report Manager (Datamension Corp.), pp. 94-101.

List

Vol. 2, No. 7, July 1984:

Special section entitled "The Best Business Software." Articles include "The First Annual *List* 101," "The Shape of Things to Come," "Accounting Software," "Communications Software," "Database Software," "Education/Training Software," "Graphics Software," "Integrated Software," "Spreadsheet Software," "Vertical/Miscellaneous Software," "Word Processing Software," and "Ranking of the 101," pp. 46-74.

Macworld

Vol. 1, No. 3, July/Aug. 1984:

K. Rietmann, "Smoothing the Critical Path" [business management software package, MacProject], pp. 52-63.

P. Hoffman, "The Word From Microsoft," pp. 72-82.

Microprocessors and Microsystems

Vol. 8, No. 4, May 1984:

D. Hutchison and D. Coffield, "Simple Token-Ring Local-Area Network," pp. 171-176.

N. F. Scholes, G. Morgan, and P. K. Lala, "Redefinable Crossassembler for Horizontally Microprogrammable Processors," pp. 177-181.

O. R. Omotayo, "Human Factors Aspects of Designing Computer Voice Output Systems as Communication Aids for the Disabled," pp. 183-188.

M. F. Smith, "Simple Multiplexed Interface for the MC6809 and the 146818 RTC," pp. 189-191.

"Hitachi HD68P05 and HD68P01 8-Bit Single-Chip Microcomputers With EPROM on the Package," pp. 196-199.

Mini-Micro Systems

Vol. 17, No. 8, June 15, 1984:

"Computer Digest" [product guides on single-board microcomputers, single-user microcomputer systems, multiuser microcomputer systems, minis, and OEM computers], pp. 17-138.

Vol. 17, No. 9, July 1984:

L. Valigra, "Hardware Differences Can Make or Break the 50 IBM PC-Compatible Manufacturers," pp. 97-104.

C. Rook, "Sampling Digitizer Produces Broadcast-Quality Messages," pp. 145-154.

C. Warren, "Graphics Software Schemes Enhance Peripheral Interfacing," pp. 163-178.

D. Simpson, "Desktop Plotters Draw Attention via Price Cuts, Color," pp. 185-216.

P. Sniger, "Mid-Range CAD/CAM/CAE Systems Dominate Graphics Display Terminals," pp. 223-252.

Vol. 17, No. 10, Aug. 1984:

C. Bailey, "Virtual Microsystems Adds PC-DOS Compatibility to DEC Micros," pp. 54-58.

R. Fosheim and D. R. Grundman, "Single-Board Computer Merges 8-, 16-Bit Performance," pp. 159-166.

R. Dalrymple, "Eurocard/DIN Single-Board Computers Signal Era of International Standards," pp. 171-178.

C. Warren, "Mature Software Tools Speed Development Tasks," pp. 183-191.

C. J. Christopher, "HP's Model 9000: Squeezing a Mainframe Into a Shoe Box," pp. 217-230.

PC

Vol. 3, No. 16, Aug. 21, 1984:

Series of short articles on robotics and process control includes: "Programming Factory Robots With PCs," "PCs, Peptides, and Process Control," "A Computerized Notebook for Scientists," "A Personal Robot Goes to Market," and "The PC Interfaces With a HERO," pp. 120-157.

S. Stallings, "Project Data Base: Part 6—Condor 3, dBase II, Mag/base III, RL-1 Data Base, Optimum, and Day One," pp. 169-206.

D. McManigal, "Adapting Your Display for Speedy Updates," pp. 225-236.

D. Holzman, "Using MS Fortran on the PC," pp. 255-264.

PC World

Vol. 2, No. 9, Aug. 1984:

H. Miller, "Introduction to Spreadsheets," pp. 66-75.

A. K. Runchal, J. Treger, and C. K. Tam, "Pick of the Plotters," pp. 132-142.

J. Martin, "Media Conversion," pp. 230-236.

S. D. Ryals, "CP/M to DOS," pp. 242-244.

C. Hamburger, "60-Second Slides," p. 267.

Vol. 2, No. 10, Sept. 1984:

J. Martin, "Laser Printers," pp. 82-91.

M. Shinyeda, "The Real Jack2 Challenge," pp. 120-127.

B. Dauphinais and L. Darnell, "Task Force" [Gantt management software], pp. 135-148.

L. Jordan, "Intelligent Communications," pp. 166-177.

N. Goodban and K. Hakuta, "Statistical Quintet," pp. 186-195.

Scientific American

Vol. 251, No. 3, Sept. 1984:

Special issue on computer software. Articles include: "Computer Software," "Data Structures and Algorithms," "Programming Languages," "Operating Systems," "Computer Software for Working With Language," "Computer Software for Graphics," "Computer Software for Information Management," "Computer Software for Process Control," "Computer Software in Science and Mathematics," and "Computer Software for Intelligent Systems," pp. 52-213.

Systems and Software

Vol. 3, No. 7, July 1984:

A. Schreyer, "Strong Bus Standards Harness CPU Explosion," pp. 71-74.

W. Rauch-Hindin, "Language System Emulates Nature," pp. 93-100.

M. Chester, "Data Communications," pp. 104-119.

J. Little, "An OS That Offers Everything" [S1 operating system], pp. 121-126.

R. J. Dickie, "Linking at the Mainframe," pp. 130-136.

R. Larribeau, Jr., "Linking at the Micro," pp. 138-144.

M. C. Budzinski, "Bitbus Promises to Standardize Control," pp. 149-153.

D. Swee, "ISO OSI Protocols in Unix Environments," pp. 167-172.

G. S. Sidhu and R. F. Andrews, "Hooking Into Applebus," pp. 173-180.

R. Baird and P. S. Bolton, "Distributed Files for CP/M, PC-DOS," pp. 183-189.

F. W. Porretto, "Real-Time Software Engineering Finds a Tool in Personal Computers," pp. 189-193.

N. Somos, "Coprocessors Enhance PC Functionality," pp. 194-200.

Vol. 3, No. 8, Aug. 1984:

R. Bernhard, "Robotics—Too Many Vendors, Too Few Applications," pp. 73-74.

J. McLeod, "Special Report: Graphics," pp. 82-94.

Y. P. Chien, "HLL Code Debugged via Simulation," pp. 97-100.

R. S. Lim, "Virtual Memory via Segmented Pages," pp. 103-106.

J. Spoerl, "AI Environment Speeds Software Development," pp. 111-118.

G. von Limbach and M. B. Taylor, "Expert System Rules Read Natual Language," pp. 119-125.

Addresses of publishers

Business Computer Systems
Cahners Publishing Co.
270 St. Paul St.
Denver, CO 80206
(303) 388-4511
(Publisher does not sell back issues or single copies of articles. Subscriptions are free to qualified readers.)

Byte
Byte Publications Inc.
70 Main St.
Peterborough, NH 03458
(603) 924-9281

Communications of the ACM
Association for Computing Machinery
11 W. 42nd St.
New York, NY 10036
(212) 869-7440

Computer
IEEE Computer Society
10662 Los Vaqueros Cir.
Los Alamitos, CA 90720
(714) 821-8380

Computer Design
Computer Design Publishing Co.
11 Goldsmith St.
Littleton, MA 01460
(617) 486-8944

Data Communications
McGraw-Hill Publications Co.
1221 Ave. of the Americas
New York, NY 10020
(212) 512-3139

Datamation
Technical Publishing Co.
1301 S. Grove Ave.
Barrington, IL 60010
(312) 774-8115

Dr. Dobb's Journal
People's Computer Co.
Box E
1263 El Camino Real
Menlo Park, CA 94025
(415) 323-3111

EDN
Cahners Publishing Co.
270 St. Paul St.
Denver, CO 80206
(303) 388-4511

Electronic Design
50 Essex St.
Rochelle Park, NJ 07662
(201) 843-0550

Electronics and *Electronics Week*
McGraw-Hill Publications Co.
1221 Ave. of the Americas
New York, NY 10020
(212) 512-2000

Elektor
Elektor Publishers Ltd.
6 Stour St.
Canterbury CT1 2XZ UK

Hewlett-Packard Journal
Hewlett-Packard Co.
3000 Hanover St.
Palo Alto, CA 94304
(415) 857-3853

IEEE Circuits and Systems Magazine
IEEE Service Center
445 Hoes Lane
Piscataway, NJ 08854
(201) 981-0060, x133

IEEE Communications Magazine
IEEE Service Center
445 Hoes Lane
Piscataway, NJ 08854
(201) 981-0060, x133

IEEE Computer Graphics and Applications
IEEE Computer Society
10662 Los Vaqueros Cir.
Los Alamitos, CA 90720
(714) 821-8380

IEEE Design & Test
IEEE Computer Society
10662 Los Vaqueros Cir.
Los Alamitos, CA 90720
(714) 821-8380

IEEE Spectrum
IEEE Service Center
445 Hoes Lane
Piscataway, NJ 08854
(201) 981-0060, x133

IEEE Transactions
IEEE Service Center
445 Hoes Lane
Piscataway, NJ 08854
(201) 981-0060, x133

Infosystems
Hitchcock Publishing Co.
Hitchcock Bldg.
23 W. 550 Geneva Rd.
Wheaton, IL 60187
(312) 665-1000

Interface Age
McPheters, Wolfe & Jones
16704 Marquardt Ave.
Cerritos, CA 90701
(213) 926-9540

List
Redgate Publishing Co.
3381 Ocean Dr.
Vero Beach, FL 32963
(305) 231-6904

Macworld
555 De Haro St.
San Francisco, CA 94107
(415) 861-3861

Microprocessors and Microsystems
Business Press International
205 E. 42nd St., Suite 1705
New York, NY 10017
(212) 867-2080

or

Butterworth Scientific Ltd.
Journals Division
PO Box 63
Westbury House
Bury St.
Guildford, Surrey GU2 5BH UK

Mini-Micro Systems
Cahners Publishing Co.
270 St. Paul St.
Denver, CO 80206
(303) 388-4511

MIT Press
28 Carleton St.
Cambridge, MA 02142
(617) 253-2884

Osborne/McGraw-Hill
630 Bancroft Way
Berkeley, CA 94710
(800) 227-2895,
in CA (415) 548-2805

PC
Software Communications, Inc.
1528 Irving St.
San Francisco, CA 94122
(415) 753-8088

PC World
555 De Haro St.
San Franciso, CA 94107
(415) 861-3861

Reston Publishing Co., Inc.
11480 Sunset Hills Rd.
Reston, VA 22090
(703) 437-8900

Scientific American
415 Madison Ave.
New York, NY 10017
(212) 754-0550

Systems and Software
Hayden Publishing Co., Inc.
50 Essex St.
Rochelle Park, NJ 07662
(201) 843-0550

ADVERTISER/PRODUCT INDEX

October 1984

Advertisers

Products

	RS#	Page#
BOARDS		
File transfer	8	75
Single-board computer	36,37	81
VME-bus-compatible microprocessor	9	76
CIRCUITS/COMPONENTS		
Cables	4	74
Chips/components	30,35	80
EPROM	10	76
Tape controllers	47	82
CONFERENCES		
Call for papers		Cover IV
I/O-RELATED EQUIPMENT		
Color card converter	41	81
DMA controller	5	75
Digital optical memory disk recorder	1	73
Emulator	42,46	81,82
Printer	45	82
Printer adapter	49	82
OTHER PRODUCTS & SERVICES		
Peripherals market research	17	79
Computer Society membership		Cover I
SOFTWARE		
Boolean construction operations extension	14	78
Ladder diagram editor	15	79
Mouse-based color graphics package	6	75
Operating system	43	82
Printer driver	45	82
Voice mail	7	78
SYSTEMS		
Artificial intelligence	12	77
Benchmark	16	79
Database management	2	73
Data acquisition	50	82
In-circuit emulator	48	82
Microcomputer	11,38,39,40	77,81
VLSI design	3	74
Workstation	13	4,5,78

FOR DISPLAY ADVERTISING INFORMATION CONTACT

Southern California and Mountain States: Richard C. Faust Company, 24050 Madison Street, Suite 100, Torrance, CA 90505; (213) 373-9604.
Northern California and Pacific Northwest: Don Farris Company, 161 W. 25th Ave., #102B San Mateo, CA 94403; (415) 349-2222.
Jack Vance, P.O. Box 3205, Saratoga, CA 95070, (408) 741-0354
East Coast: Hart Associates, Inc., P.O. Box 339, 42 Lake Blvd., Matawan, NJ 07747; (201) 583-8500.
New England: Arpin Associates, P.O. Box 227, Weston, MA 02193; (617) 899-5613.
George Watts, III, 4 Conifer Dr., Wilbraham, MA 01095; (413) 596-4747.
Midwest: Jerry Berk, Special Market Media, 421 Florence Ave., Evanston, IL 60202; (312) 271-2001.
Southeast: Larry C. Shattles, 133 Laurel Oak Drive, Longwood, FL 32779; (305) 788-1950
Southwest: The House Company, 3817 Richmond Avenue, Suite 110, Houston, TX 77027; (713) 622-2868.

Advertising Director: Mike Koehler, *IEEE MICRO*, 10662 Los Vaqueros Circle, Los Alamitos, CA 90720, (714) 821-3240, 821-8380,

For production information, conference or classified advertising contact Jonne Marriott, *IEEE MICRO*, 10662 Los Vaqueros Circle, Los Alamitos, CA 90720, (714) 821-1140.

IEEE MICRO READER SERVICE

For further information on advertised products, new products, or literature, fill out one of these cards. Circle the number on the Reader Service Card that corresponds to the number at the bottom of the item in which you are interested. Affix stamp and mail.

Please print or type your name and address.

READER SERVICE CARD

IEEE MICRO

Void after April 15, 1985 **10/84**

Name _____

Company _____

Address _____

City _____ State _____ Zip _____

Title _____

Telephone number ( ) _____

101 ☐ Please send me the IEEE CS *Publications Catalog.*

102 ☐ Please send me an IEEE fellows nomination form.

Articles I liked in this issue:

A ○ Guest Editor's Intro. (p. 7)
B ○ Micro Peripherals (p. 9)
C ○ Non-Death of Paper (p. 18)
D ○ New Peripheral for 3D Input (p. 26)
E ○ On-line Script Recognition (p. 36)
F ○ Smart Digital-Readout Circuit (p. 44)
G ○ Motorola's Micros (p. 55)
H ○ Microreview (p. 64)
I ○ Microlaw (p. 66)
J ○ Microstandards (p. 69)
K ○ New Products (p. 73)
L ○ Product Summary (p. 80)
M ○ Access (p. 83)

PRODUCTS PURCHASED OR SPECIFIED	FOR JOB	FOR HOBBY
Computer	☐	☐
Peripherals	☐	☐
Data communications	☐	☐
Memories, components	☐	☐
Software and services	☐	☐
Publications	☐	☐
Other	☐	☐

Send more information on numbered items:

1	5	9	13	17	21	25	29	33	37	41	45	49	53	57	61	65	69	73	77	81	85	89	93	97
2	6	10	14	18	22	26	30	34	38	42	46	50	54	58	62	66	70	74	78	82	86	90	94	98
3	7	11	15	19	23	27	31	35	39	43	47	51	55	59	63	67	71	75	79	83	87	91	95	99
4	8	12	16	20	24	28	32	36	40	44	48	52	56	60	64	68	72	76	80	84	88	92	96	100

READER SERVICE CARD

IEEE MICRO

Void after April 15, 1985 **10/84**

Name _____

Company _____

Address _____

City _____ State _____ Zip _____

Title _____

Telephone number ( ) _____

101 ☐ Please send me the IEEE-CS *Publications Catalog*

102 ☐ Please send me an IEEE fellows nomination form.

Articles I liked in this issue:

A ○ Guest Editor's Intro. (p. 7)
B ○ Micro Peripherals (p. 9)
C ○ Non-Death of Paper (p. 18)
D ○ New Peripheral for 3D Input (p. 26)
E ○ On-line Script Recognition (p. 36)
F ○ Smart Digital-Readout Circuit (p. 44)
G ○ Motorola's Micros (p. 55)
H ○ Microreview (p. 64)
I ○ Microlaw (p. 66)
J ○ Microstandards (p. 69)
K ○ New Products (p. 73)
L ○ Product Summary (p. 80)
M ○ Access (p. 83)

PRODUCTS PURCHASED OR SPECIFIED — FOR JOB — FOR HOBBY
Computer ☐ ☐
Peripherals ☐ ☐
Data communications ☐ ☐
Memories, components ☐ ☐
Software and services ☐ ☐
Publications ☐ ☐
Other ☐ ☐

Send more information on numbered items:

1 5 9 13 17 21 25 29 33 37 41 45 49 53 57 61 65 69 73 77 81 85 89 93 97
2 6 10 14 18 22 26 30 34 38 42 46 50 54 58 62 66 70 74 78 82 86 90 94 98
3 7 11 15 19 23 27 31 35 39 43 47 51 55 59 63 67 71 75 79 83 87 91 95 99
4 8 12 16 20 24 28 32 36 40 44 48 52 56 60 64 68 72 76 80 84 88 92 96 100

Comments on articles and other editorial matter

I liked: _____

_____

_____

_____

_____

I disliked: _____

_____

_____

I would like: _____

_____

_____

_____

For reader service, see other side

This PO box for reader service cords only.

PLACE STAMP HERE

IEEE MICRO

Reader Service Inquiries
Box 24168
Los Angeles, CA 90024
USA

Comments on articles and other editorial matter

I liked: _____

_____

_____

_____

_____

I disliked: _____

_____

_____

I would like: _____

_____

_____

_____

For reader service, see other side

This PO box for reader service cords only.

PLACE STAMP HERE

IEEE MICRO

Reader Service Inquiries
Box 24168
Los Angeles, CA 90024
USA

PROFESSIONAL CALENDAR

February 1985

Fourth Annual IEEE Computer Faire, February 22-23, Huntsville, Alabama. Contact Terry Mizell, PO Box 5188, Huntsville, AL 35805; (205) 532-2036.

Compcon Spring 85, Technological Leverage: A Competitive Necessity, February 25-28, San Francisco, California. Contact Glen G. Langdon, Jr., IBM Corp. K54-282, 5600 Cottle Rd., San Jose, CA 95193; (408) 256-6454.

March 1985

Workshop on Personal Computer and STD Computer Interfacing for Scientific Instrument Automation, March 14-16, Blacksburg, Virginia. Contact Linda Leffel, C.E.C., Virginia Polytechnic Institute and State University, Blacksburg, VA 24061; (703) 961-4848.

PCCC 85, Fourth Annual Phoenix Conference on Computers and Communications, March 20-22, Phoenix, Arizona. Contact IEEE PCCC-85, PO Box 37125 C, Phoenix, AZ 85069.

Comdex Winter, March 21-24, Anaheim, California. Contact The Interface Group, 300 First Ave., Needham, MA 02194; (617) 449-6600.

IEEE Infocom 85, Computers and Communications Integration: The Confluence at Mid-Decade, March 25-28, Washington, DC. Contact John Daigle, University of Rochester, Rochester, NY 14627; (716) 275-4791.

1985 IEEE International Conference on Robotics and Automation, March 25-28, St. Louis, Missouri. Contact K. S. Fu, Electrical Engineering Dept., Purdue University, West Lafayette, IN 47907; (317) 494-3433.

Tutorial Week East, March 25-29, Lake Buena Vista, Florida. Contact Tutorial Week East, PO Box 639, Silver Spring, MD 20901; (301) 589-8142; TWX 7108250437 IEEECOMPSO.

Comdex in Japan, March 26-28, Tokyo, Japan. Contact The Interface Group, Inc., 300 First Ave., Needham, MA 02194; (617) 449-6600.

First International Workshop on Current Issues and Future Directions in Microprogramming (ACM), March 26-29, Colorado Springs, Colorado. Contact Robert A. Mueller, Computer Science Dept., Colorado State University, Fort Collins, CO 80523; (303) 491-5792.

Softcon International Conference and Trade Fair for Software Merchandisers, Publishers, and Corporate and Institutional Users, March 31-April 3, Atlanta, Georgia. Contact Northeast Expositions, 822 Boylston St., Chestnut Hill, MA 02167; (617) 739-2000.

April 1985

1985 IEEE VLSI Test Workshop, Microsystem Test Challenges, April 1-2, Atlantic City, New Jersey. Contact Bob Tigue, IBM Dept. 69J/422, Neighborhood Rd., Kingston, NY 12401; (914) 385-7440.

IEEE Microprocessor Forum 85, Pathways to Design Productivity, April 2-4 (tutorials to be offered March 31-April 1), Atlantic City, New Jersey. Contact Helen Yonan, IEEE Office, Moore School of Electrical Engineering, University of Pennsylvania, Pittsburgh, PA 19104; (215) 898-8106.

Speech Tech 85, Voice Input/Output Applications Show, April 22-24, New York, New York. Contact Stanley Goldstein, Media Dimensions, Inc., PO Box 1121 Gracie Station, New York, NY 10028; (212) 772-7068 or (212) 680-0451.

May 1985

1985 Spring Workshop of the Computer Society Technical Committee on Packaging, May 1-3, Palm Desert, California. Contact Ray Usell, Burroughs Corp., PO Box 28810, San Diego, CA 92128; (619) 451-4397.

ACM Symposium on Small Systems, May 2-3 (tutorials on May 1), Danvers, Massachusetts. Contact Fred Maryanski, EECS Dept., U-157, University of Connecticut, Storrs, CT 06268.

Comdex Spring, May 6-9, Atlanta, Georgia. Contact The Interface Group, Inc., 300 First Ave., Needham, MA 02194; (617) 449-6600.

Fifth International Conference on Distributed Computing Systems, May 13-17, Denver, Colorado. Contact Earl Swartzlander, TRW (02/2791), 1 Space Park, Redondo Beach, CA 90278; (213) 535-4177.

1985 Chapel Hill Conference on VLSI, May 15-17, Chapel Hill, North Carolina. Contact Henry Fuchs, Dept. of Computer Science, New West Hall 035A, University of North Carolina, Chapel Hill, NC 27514; (919) 966-4650.

CICC 85, Custom Integrated Circuits Conference (IEEE), May 20-22, Portland, Oregon. Contact Aris K. Silzars, Tektronix, Inc., PO Box 500 MS 13-800, Beaverton, OR 97077; (503) 627-6980.

June 1985

12th International Symposium on Computer Architecture (ACM), June 17-19, Boston, Massachusetts. Contact Tilak Agerwala, IBM Research, PO Box 218, Yorktown Heights, NY 10598.

FTCS-15, 15th International Symposium on Fault-Tolerant Computing, June 19-21, Ann Arbor, Michigan. Contact John F. Meyer, Dept. of Electrical Engineering and Computer Science, 1075 E. Engineering Bldg., The University of Michigan, Ann Arbor, MI 48109; (313) 763-0037; telex 810-223-6056.

DAC 85, 22nd Design Automation Conference (ACM), June 23-26, Las Vegas, Nevada. Contact Hillel Ofek, Silvar-Lisco, 1080 Marsh Rd., Menlo Park, CA 94025; (415) 324-0700.

July 1985

NCC 85, National Computer Conference (ACM, AFIPS, DPMA, SCS), July 15-18, Chicago, Illinois. Contact AFIPS, 1899 Preston White Dr., Reston, VA 22091; (703) 620-8900.

August 1985

CHDL 85, IFIP Seventh International Symposium on Computer Hardware Description Languages and Their Applications (ACM), August 26-31, Tokyo, Japan. Contact Tohru Moto-oka, Dept. of Electrical Engineering, University of Tokyo, Hongo, 7 Chome, Bunkyo-ku, Tokyo, Japan; phone 812 2111, ext. 6652.

October 1985

ICCD 85, International Conference on Computer Design: VLSI in Computers, October 7-10, Port Chester, New York. Contact ICCD 85, PO Box 639, Silver Spring, MD 20901; (301) 589-8142; telex 7108250437 IEEECOMPSO.

CALL FOR PAPERS and Participation

San Jose Convention Center
San Jose, California
November 11–14, 1985

Sponsored by:

IEEE COMPUTER SOCIETY®

1st INTERNATIONAL CONFERENCE ON COMPUTER WORKSTATIONS

COMPUTER WORKSTATIONS are integral to increases in productivity and quality, and they are the main focal point for a growing fraction of professional activity.

A "workstation," broadly defined, is a system that supports a user accomplishing some kind of work. Included in this definition are: CAD systems, high-resolution graphics systems, office productivity systems, computer-based engineering support stations of all kinds, architectural systems, software engineering environments, etc.

Workstations include both hardware and software — hardware to run the applications, and software to customize the environment to an application.

Papers are solicited from the technical community at large.

Within a broad definition of "computer workstations," the following topics are included in the conference: workstation hardware from PC's (used for professional/commercial tasks) to larger CAD workstations, hardware and software subsystems that are different from mainframe subsystems, e.g., graphics displays, mice, window managers, LAN's miniwini's, personal printers, spreadsheets, WYSIWYG editors. Included are operating systems, e.g., UNIX; loosely coupled networks, and applications that are made possible via workstation technology, e.g., technical document systems, interactive graphics systems for CAD for ME's, CE's, EE's, architects, cartographers, aerospace E's, and of course software people. Of particular interest are user-computer interfaces that extend beyond terminals, and distributed systems based on workstation hardware/software.

This conference covers a wide range of topics but is not all inclusive. For example, the following topics are not likely to be suitable: centralized database systems, home computers (PCjr, Apple II, Comm.) host dependent terminals (a significant amount of the application code must run on the workstation to qualify), computer peripherals (disks, tapes, printers, but print servers on a network would be suitable). Several other topics are important, but not suitable either: mainframe-based project management software, business software (COBOL based applications), centralized voice/mail systems, and mainframe operating systems.

Send four copies of a paper not exceeding 25 double-spaced pages by May 1, 1985, to the Program Co-Chairmen, Dr. Robin Williams and Dr. Patrick Mantey, at the following address:

Dr. Robin Williams
IBM Research
K52 — 282
5600 Cottle Road
San Jose, CA 95193
Phone: (408) 256-3859

Papers will be refereed. Those accepted will be limited to five camera-ready pages and will be bound into a proceedings to be distributed at the conference.

Over 150 booths are expected to be populated by companies exhibiting hardware and software or workstations of all kinds. High standards of technical exhibitions will be maintained by the IEEE to assure a technically sophisticated and educational set of exhibits. International participation is anticipated.

For further information about exhibits, contact the General Chairman:

Dr. Edward Miller
Software Research, Inc.
580 Market Street
San Francisco, CA 94104
Phone: (415) 957-1441
Telex: 340 235

THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, INC.®